TECHNICAL UNIVERSITY OF MOMBASA

School of Engineering and Technology

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION 2024/2025

BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 4409: DIGITAL SYSTEMS DESIGN I

TIME: 2 HOURS **SERIES:** March, 2025

INSTRUCTIONS TO CANDIDATES

1. You are required to have the following for this examination;
   - Answer Booklet
   - A non- Programmable Calculator
2. Answer **ANY THREE** Questions.

Question ONE

(a) (i) State the design procedures for a combinational logic circuit.

(ii) Design a logic circuit that takes a 2-bit number and obtains its square. Implement using NOR gates **(8 marks)**

(b) Design a logic circuit that has an enable input 'E' such that it converts a 3-bit gray code to its equivalent 3-bit binary value when E = 0 and when E = 1, it converts a 3-bit binary value to its gray code equivalent. Implement using appropriate encoder and decoder with minimum external IC package. **(12 marks)**

Question TWO

a) Obtain a minimum SOP expression for the function below using the abbreviated binary method of tabular minimization. (**10 marks**)
$F(A,B,C,D,E) = \sum_m(1, 5, 9, 10, 11, 12, 13, 14, 17, 21, 25, 26, 27, 28, 29, 30)$

b) Design a code converter that translates Excess-3 BCD to 8421BCD. Implement using PLA. (**10 marks**)

QUESTION THREE

a) Develop a full ADDER using NAND gates. (**11 marks**)

b) An electronic thermometer, designed for greenhouse use, has a 5-bit binary output representing a temperature range from 0^0C to 31^0C. A plug-in logic module is to be designed to output logic **1** when the temperature is even below and odd above 7^0C. Design the following gate combinational networks to implement this specification:

i) OR-to-NAND and

ii) NOR-to-NOR. Comment on the two designs. (**9 marks**)

QUESTION FOUR

a) Obtain logic diagram for a 4-to-2 priority encoder for the following available signals ~F_1[NL], F_0, I_3, ~I_2[NL], I_1, I_0. (**5 marks**)

b) Given the state diagram in Figure Q4, generate the state table and design a sequence circuit using T-flip flops. (**10marks)**

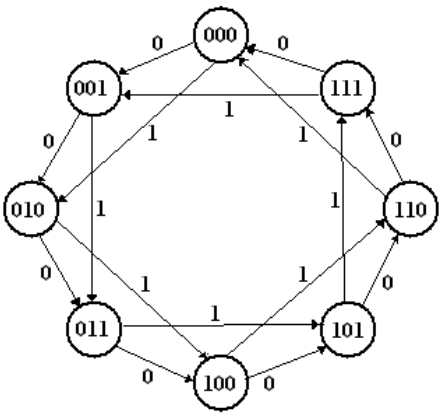

Figure Q4

c) Using a 4 – to – 1 multiplexer, implement the function

$\mu f(A,B,C,D) = \sum_m (0,\ 2,\ 4,\ 7,\ 8,\ 10,\ 11, 12,\ 14, 15)$. **(5 marks)**

QUESTION FIVE

a) Explain the general technique to design a divide by N ripple counter, assuming J-K flip-flops with preset available. (**5 marks**)

b) With aid of a transition table, design a modulo-6 T flip-flop based synchronous counter to repetitively count in the sequence 0, 1, 2, 3, 4, 5, 0…. The unused states will assume a value represented by 3. Other than the flip-flop IC packages, determine the minimum number of IC packages. (**15marks)**