TECHNICAL UNIVERSITY OF MOMBASA

School of Engineering and Technology

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION 2023/2024

BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 4409 : DIGITAL SYSTEMS DESIGN I

TIME: 2 HOURS **SERIES:** August, 2024

INSTRUCTIONS TO CANDIDATES

1. You are required to have the following for this examination;
   - Answer Booklet
   - A non-Programmable Calculator
2. This paper consists of **FIVE** Questions.
3. Answer **Question ONE and any other TWO** Questions.

Question ONE (Compulsory)

a) Design a code converter that translates a 3-bit gray code to its corresponding binary value. Implement using 4 – to – 1 Multiplexers with minimum external circuitry. (1**2 marks**)

b) With aid of a transition table, design a J-K flip-flop based synchronous counter to repetitively count in the sequence 5, 4, 3, 2, 1, 0, 5 …. The unused states will assume a value represented by 4 after a trigger pulse. Other than the flip-flop IC packages, determine the minimum number of IC packages. (**18marks)**

Question TWO

a) Describe the Finite State Machine design procedures. (**6 marks**)

b) A Finite State Machine is used to control a vending machine that delivers a packet of juice after it has received thirty shillings in coins. The machine has a single coin slot that accepts ten shilling and twenty-shilling coins, one at a time. A mechanical sensor indicates to the control whether a ten or a twenty-shilling coin has been inserted into the coin slot. The controller's output causes a single packet of juice to be released to the customer. The machine does not give change. The coin sensor returns any coins it does not recognize, and an external logic is used to reset the machine after the packet of juice is delivered

   i) Draw a block diagram to represent the vending machine,

ii) List the sequences that lead to release of a packet of juice,
iii) Represent the sequences with a simplified state diagram
iv) Develop an encoded state transition table for the vending machine assuming D flip-flops are used. (**14 marks**)

Question THREE

a) Implement a full subtractor using NOR gates. (**10 marks**)

b) Derive the state table and the state diagram of the sequential circuit shown in Figure Q3. (**10 marks**)

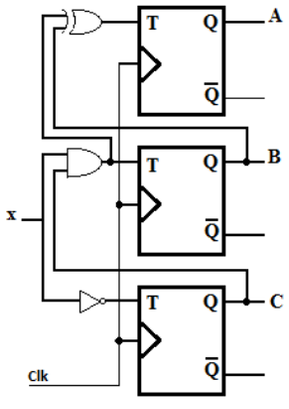

Figure Q3

Question FOUR

a) Explain the functions of the following digital devices:
i) Multiplexer,
ii) Decoder,
iii) Binary Comparator. (**6 marks**)

b) A circuit that controls a given digital system has three inputs: *x*, *y* and *z*. It has to recognize three different conditions:
Condition A is true if *x* is true and either *y* or *z* is false.
Condition B is true if *y* is true and either *x* is true or *z* is false.
Condition C is true if *z* is true and either *x* is true or *y* is false.
The control circuit must produce an output of 1 if at least two of the conditions A, B and C are true. Design the simplest circuit that can be used for this purpose. (**9 marks**)

c) Obtain realizable logic diagram for a 4-to-2 priority encoder for the following available signals ~F_1[NL], F_0, ~I_2[NL], I_1, I_0. (**6 marks**)

Question FIVE

a) Given two 2-bit binary numbers A_1A_0 and B_1B_0, design a PLA device to implement a magnitude comparator to produce outputs when the first number is 'equal to', 'less than' and 'greater than' the second number. (**14 marks**)

b) Determine the size of the PROM required for implementing the following logic circuits:
i. a binary multiplier that multiplies two four-bit numbers;
ii. a dual 8-to-1 multiplexer with common selection inputs; and

iii. a single-digit BCD adder/subtractor with a control input for selection of operation. (**6 marks**)