



TECHNICAL UNIVERSITY OF MOMBASA

School of Engineering and Technology

Department of Electrical and Electronic Engineering

UNIVERSITY EXAMINATION FOR:

Bachelor of Science in Electrical and Electronic Engineering

EEE 4407: Digital Systems Design II

END OF SEMESTER EXAMINATION

SERIES: JULY 2025

TIME: 2 HOURS

DATE: July 2025

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **five** Questions; Question ONE is compulsory. In addition, attempt any Other TWO Questions.

Do not write on the question paper.

Question ONE (Compulsory 30 marks)

- a) Design using ASM, digital system with two flip-flops, E and F, and 4 – bit binary counter, A. The individual flip-flops in A are denoted by A_4 , A_3 , A_2 and A_1 , with A_4 holding the most significant bit of the count. A start signal S initiates the system operation by clearing the counter A and flip-flop F. The counter is then incremented by 1 starting from the next clock pulse and continues to increment until the operations stop. Counter bits A_3 and A_4 determine the sequence of operations:
- i) If $A_3 = 0$, E is cleared to 0 and the count continuous
 - ii) If $A_3 = 1$, E is set to 1; then $A_4 = 1$, F is set to 1 on the next clock pulse and the system stops counting.
- [10 marks]
- b) Develop the register-transfer logic notation with three 16-bit register AR, BR and CR that perform the following operations:
- (i) Transfer two 16-bit signed numbers (in 2's complement to AR and BR
 - (ii) If the number in AR is negative, divide the number in AR by 2 and transfer the result to register CR

- (iii) If the number in AR is positive but non zero, multiply the number in BR by 2 and transfer the result to CR
- (iv) If the number in AR is zero, clear register CR to 0

[8 marks]

- c) State any TWO types of micro-operations encountered in digital systems. [2 marks]
- d) Using full adder and associated combinational logic circuits of Figure Q1(b), design a 3 – bit arithmetic circuit to perform the following:
 When $S = 0$ the circuit performs $F_i = A_i + B_i$
 When $S = 1$ the circuit performs $F_i = A_i + \overline{B_i} + 1$ [10 marks]

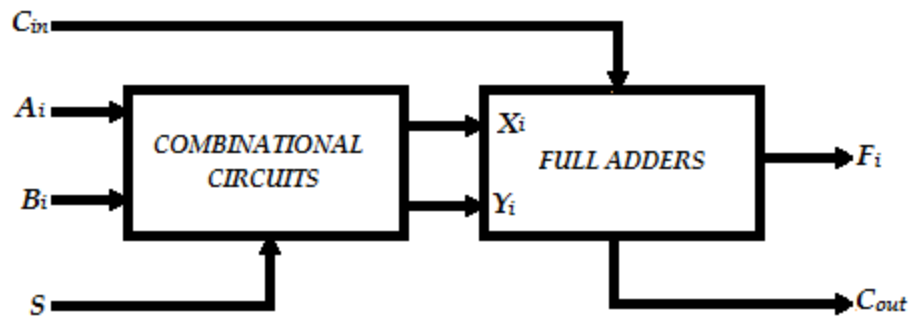


FIG. Q1(b)

Question TWO

- a) With the aid of a block diagram describe the following control logic organisations:
 - i) PLA control
 - ii) Micro-program control [10 marks]
- b) A processor unit employs a scratchpad memory. The processor consists of 64 registers of eight bits each. Determine
 - i) The size of the scratchpad memory
 - ii) The number of lines needed for the address
 - iii) The number of lines the input data. [5 marks]
- c) i) Show the block diagram of the hardware that implements the following register transfer statements.

$$YT_2: R3 \leftarrow R2, R2 \leftarrow R3$$

- ii) State what is wrong with the following register transfer statements

$$I \ xT: AR \leftarrow AR, AR \leftarrow 0$$

$$II \ yT: R1 \leftarrow R2, R1 \leftarrow 0$$

marks]

Question THREE

- a) Determine
- i) the number of 128×8 RAM chips needed to provide a memory capacity of 2048 bytes
 - ii) the number of lines of the address bus that must be used to access 2048 bytes of memory and how many of these lines will be common to all chips
 - iii) the number of lines that must be decoded for chip select, and specify the size of the decoders

[8 marks]

- b) A typical processor unit is designed to consist of a register file with seven registers R1 through R7, two multiplexers to select bus A input and B input, a destination select decoder, an ALU and a shifter register and a status register.
- i) Draw a block diagram of processor unit with appropriate interconnection and describe its operation.
 - ii) Draw the corresponding control word diagram and describe the function of each field
 - iii) Give the bit values in the control word for the following micro-operation

I $(R1 \leftarrow R1 - R6)$

II $(R1 \leftarrow R4)$

[12 Marks]

Question FOUR

- a) Define the following:
- (i) Decoder
 - (ii) Multiplexer
 - (iii) Demultiplexer
- [3 marks]
- b) Implement
- $$F(A,B,C,D) = \sum_M (1,4,5,7,9,12,13)$$
- using a 4 – to – 1 multiplexer
- [6 marks]
- c) Draw a diagram of bus system for four registers of 4-bits each. The bus is to be constructed with multiplexers
- [4 marks]
- d) i) Differentiate between Algorithm State Machine (ASM) and conventional flow chart.
- ii) Using Figure Q4(d) interpret the events
- [7 marks]

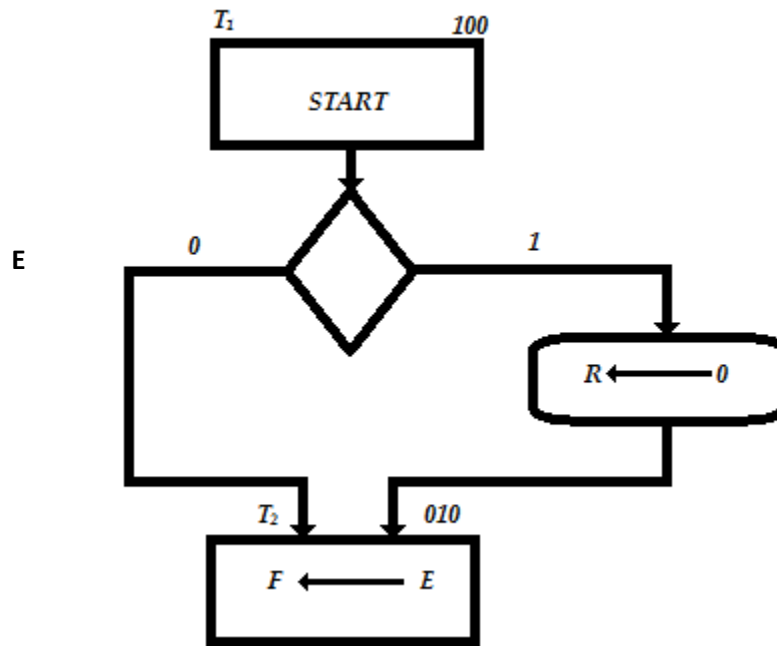


FIG. Q4(d)

Question FIVE

- Design an adder/ subtractor circuit with one selection variable, S and two inputs A and B when $S = 0$, the circuit performs $A + B$ and when $S = 1$, the circuit performs $A - B$. Draw the logic diagram of two typical stages
[14 Marks]
- With the aid of a diagram, explain the operation of a two-port scratchpad memory used by a processor unit
[6 marks]