PP1

TECHNICAL UNIVERSITY OF MOMBASA

INSTITUTE OF COMMUNICATION & INFORMATICS (ICI)

UNIVERSITY EXAMINATION FOR:

Bachelor of Technology in Information Technology(BTIT)

Bachelor of Science in Computer Science (BSIT)

Bachelor of Science in Information Technology(BSCS)

EEE4250: DIGITAL ELECTRONICS

END OF SEMESTER EXAMINATION

SERIES: APRIL 2025

TIME: 2 HOURS

DATE: April 2025

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **FIVE** Questions; Attempt Question ONE and any other TWO Questions.

Do not write on the question paper.

Question ONE (Compulsory 20 marks)

a) Define the following terms as applied to number systems ;

i) radix

ii) weight **(2marks)**

b) Perform the following conversions

I) 42.3125_{10} to binary

II) 110101.1010_2 to decimal

III) 473_8 to hexadecimal

iv) 357_8 to decimal **(6 marks)**

c) Perform the following operations

i) BA_{16} +$A5_{16}$

ii) 16_8 +34_8

iii) -18-27 using 2's complement addition

iv) 15-9 using 1's complement addition **(8marks)**

d) i) Convert $10111010101_2$to gray code

ii) Add the following two BCD Numbers

88+52 **(4 marks)**

Question TWO

a) i) An operator is typing in a BASIC program at the keyboard of a certain microcomputer.

The computer converts each keystroke into its ASCII code and stores the code in memory. Determine the codes that will be entered into memory when the operator types in the following BASIC statement; **GOTO 25**

ii) The Following ASCII coded message is stored in successive memory locations in a computer;

1010011 1010100 1001111 1010000 What is the message ? **(2 marks)**

b) i) Draw the truthtable for converting 3 bit binary code to 3 bit gray code

ii) Write the expressions for g_2 ,g_1 ¿ g_0

iii) Minimize the expressions using Karnaugh maps

iv) Draw the resulting logic circuit for the minimized expression **(10 marks)**

c) Determine

(i) the excess-3 equivalent of 237.75_{10}

(ii) the decimal equivalent of the excess-3 number 110010100011.01110101.

(2marks)

d) i) Locate the error in the following data which are being transmitted with the odd parity

Data	Row parity bit
101010	0
110101	1
011100	0
011111	0
011101	1
110110	Column parity bit

ii) A transmitter is sending ASCII coded data to a receiver with an odd parity bit. Show the actual codes when the transmitter is sending the message 'HELLO' (append the appropriate parity bit at the end of each code word). **(4 marks)**

Question THREE

a) i) Prove by truth table that ; $\overline{A.B} = \overline{A} + \overline{B}$

ii) Simplify the following logical expressions using Boolean algebra;

I) X= $\overline{A}\,\overline{C}$ +AB$\overline{C}$ +$\overline{A}$ BC+A$\overline{B}\,\overline{C}$

II) F= $\overline{A+\overline{B+C}}$ **(7 marks)**

b) Use Karnaugh map to simplify the following expression

i) F=$\overline{A}\,\overline{B}\,\overline{C}$ +A$\overline{B}\,\overline{C}$ +B$\overline{C}$ +$\overline{A}$ C

ii) F(a,b,c,d) =∑(2,3,7,8,9,10,11) **(5 marks)**

c) Implement the following Boolean expression using NAND gates only

F=$\overline{A}$ B +A$\overline{B}$ **(3 marks)**

d) i) Write the Boolean expression of figure Q 3d(i) and reduce it using Boolean identities

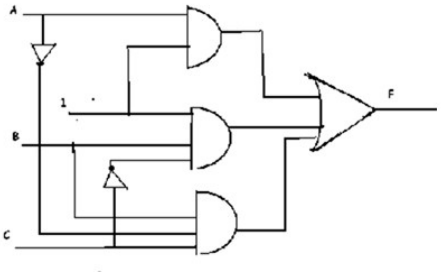

Figure Q3d

ii) Find the min-terms of F=A$\overline{B}$+$\overline{C}$ and Write the expression in the form Σ(a,b,c) **(5 marks)**

Question FOUR

a) i) Draw a diagram of a 4bit parallel adder and Explain how it is used to add the two numbers 1110 in register A and 1010 in register B

ii) With the aid of a diagram, Show how two half adders may be connected to realize a full adder **(7 marks)**

b) Design a half subtractor and Draw the logic diagram **(6 marks)**

c) Design a decimal to BCD encoder and implement it using OR gates only **(7 marks)**

Question FIVE

a) With the aid of a logic diagram and state table ,explain the operation of the leading edge triggered J-K flip flop **(8 marks)**

b) Use the negative-edge-triggered *RS* flip-flop truth table to explain *Q* changes of state with time in Figure Q5b **(4 marks)**

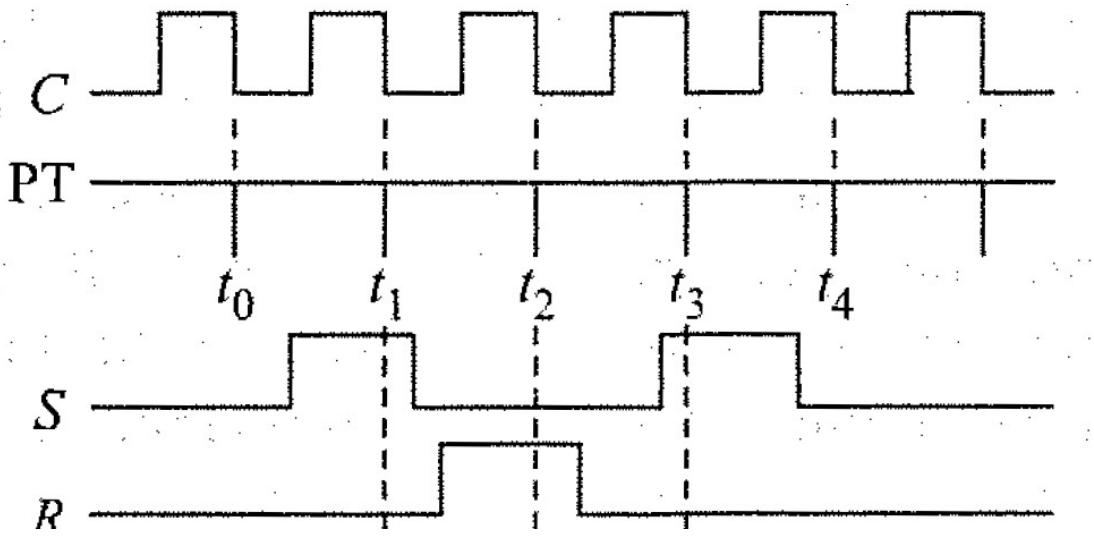

Figure Q 5b

c) Design a synchronous counter employing D Flip-flops to count in the sequence

$0 \longrightarrow 5 \longrightarrow 2 \longrightarrow 4 \longrightarrow 9 \longrightarrow 11$ **(8 marks)**

TABLE 11-6. / ASCII Code

MSB / LSB	Binary	000	001	010	011	100	101	110	111
Binary	Hex	0	1	2	3	4	5	6	7
0000	0	NUL	DEL	SP	0	@	P	`	p
0001	1	SOH	DC1	!	1	A	Q	a	q
0010	2	STX	DC2	"	2	B	R	b	r
0011	3	ETX	DC3	#	3	C	S	c	s
0100	4	EOT	DC4	$	4	D	T	d	t
0101	5	END	NAK	%	5	E	U	e	u
0110	6	ACK	SYN	&	6	F	V	f	v
0111	7	BEL	ETB	'	7	G	W	g	w
1000	8	BS	CAN	(	8	H	X	h	x
1001	9	HT	EM	)	9	I	Y	i	y
1010	A	LF	SUB	*	:	J	Z	j	z
1011	B	VT	ESC	+	;	K	[	k	{
1100	C	FF	FS	,	<	L	\	l	|
1101	D	CR	GS	-	=	M	]	m	}
1110	E	SO	RS	.	>	N	^	n	~
1111	F	SI	US	/	?	O	_	o	DEL