PP2

TECHNICAL UNIVERSITY OF MOMBASA

INSTITUTE OF COMMUNICATION & INFORMATICS (ICI)

UNIVERSITY EXAMINATION FOR:

Bachelor of Technology in Information Technology(BTIT)

Bachelor of Science in Computer Science (BSIT)

Bachelor of Science in Information Technology (BSCS)

EEE4250: DIGITAL ELECTRONICS

END OF SEMESTER EXAMINATION

SERIES: JULY 2025

TIME: 2 HOURS

DATE: July 2025

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **FIVE** Questions; Attempt Question ONE and any other TWO Questions.

Do not write on the question paper.

Question ONE (Compulsory 20 marks)

a) Define the following terms as applied to number systems ;

i) radix

ii) weight **(2marks)**

b) Perform the following conversions;

i) 38.187_{10} to hexadecimal

ii) 465_{8} to hexadecimal

iii) 11010001.101_{2}

iv) 11100101001_{gray} to binary

v) 37.6875_{10} to binary **(10 marks)**

c) Perform the following mathematical operations

i) 01010111+10000101(BCD numbers)

ii) 26_{10} -12_{10} using 1's complement

iii) 33_{10} -47_{10} using 2s component

iv) $A21_{16}$+$13B_{16}$ **(8 marks)**

Question TWO

a) i) State Demorgan's theorem

ii) Simplify the following expressions using Boolean algebra

I) F=A$\overline{B}$C+AB$\overline{C}$ +ABC

ii) F=$\overline{(\overline{A}+B)(A+\overline{B}+C)}$ **(6 marks)**

b) Minimize the following expressions using Karnaugh maps

i) F=A$\overline{C}$ D+$\overline{A}$ B$\overline{C}$ D+$\overline{A}$ $\overline{B}$ D+A$\overline{B}$ CD

ii) F=AB$\overline{C}$ +$\overline{A}$ BC+A$\overline{B}$ $\overline{C}$ +$\overline{A}$ $\overline{C}$ **(4 marks)**

c) Design a 3 bit odd parity bit generator and draw the final logic circuit (**10 marks)**

Question THREE

a) Referring to a full adder

i) Draw the truth table

ii) Using Karnaugh maps, Obtain the minimum logical expression

iii) Draw the logical circuit for the minimized expression (10 marks)

b) With the aid of a truth table implement a logic circuit that produces a 1 output only when its three input variables represent a zero, two, four ,five, six and seven(4 marks)

c) With the aid of a truth table, Draw the logic circuit of a BCD to decimal decoder (6marks)

Question FOUR

a) i) Explain the difference between a decoder and a multiplexer

ii) Explain the functions of the synchronous inputs of a flip flop (4marks)

b) Design a 4 to 1 line Multiplexer and implement the resulting Logic circuit (6 marks)

c) Draw the outputs of Figure Q4c assuming leading edge triggered flip flop (2marks)

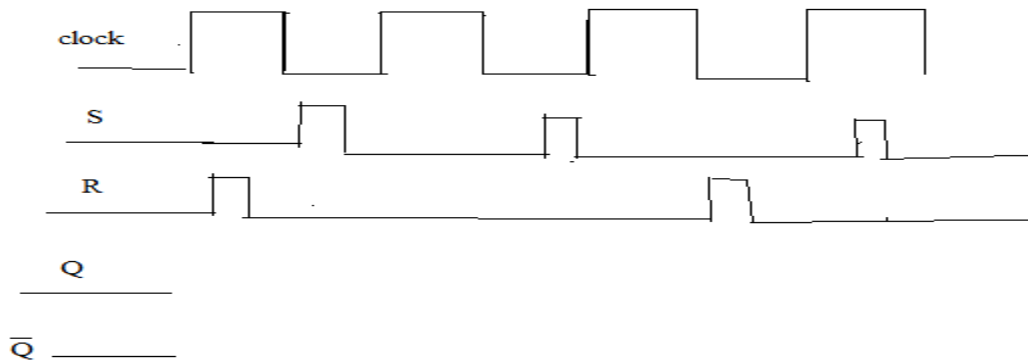

Figure Q4c

d) With the aid of a logic diagram and sequence table, explain the operation of a 4 bit serial register employing D –Flip-flops assume the data at the input is 1010**(8 marks**)

Question FIVE

a) With the aid of a circuit diagram, and sequence table explain the operation of a 3 bit Johnson counter employing D flip flops **(4marks)**

b) Design using J-K flip flops a synchronous counter to count through the states

1---2----5------7 **(6 marks)**

c) With the aid of a circuit diagram , Describe how the two numbers 11101 contained in register A and 10101 in register B are added in a parallel adder **(5 marks)**

d) Construct a ripple counter having modulo 10 **(5 marks)**