TECHNICAL UNIVERSITY OF MOMBASA

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION FOR:

Bachelor of Technology in Electrical and Electronic Engineering

TEE 4202 ANALOGUE ELECTRONICS I

END OF SEMESTER EXAMINATION

SERIES: MARCH 2025

TIME: 2 HOURS

DATE: MARCH 2025

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **FIVE** Questions; Attempt Question ONE and any other TWO Questions.

Do not write on the question paper.

Question ONE (Compulsory 20 marks)

a) i) Explain any THREE factors that affect the operating point of an amplifier
ii) State how each of the factors may be minimized **(6 marks)**

b) Referring to the potential divider bias circuit used to bias the common emitter amplifier
i) Explain how dc stabilization of the Q point is achieved in the circuit
ii) Explain the effect of leaving the emitter resistor un decoupled **(4marks)**

c) For the CE amplifier of Figure Q1c, Take V_{BE}=0.7V and β=80, determine

i) I_{BQ} ii) I_{CQ} iii) $V_{CE(Q)}$ **(3marks)**

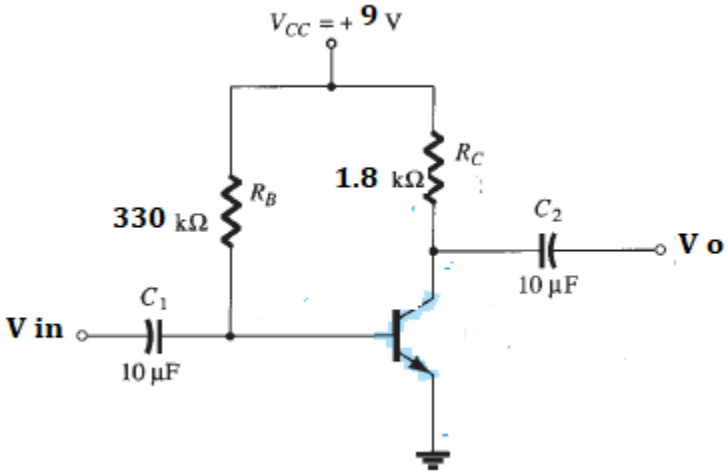

Figure Q1c

d) Draw a diagram of the NPN transistor and explain its operation **(7 marks)**

Question TWO

a) Explain what is meant by the following terms as applied to semiconductor theory
i) doping ii) extrinsic iii) intrinsic **(3 marks)**

b) Draw a diagram of a p-n unction and explain its operation **(7marks)**

c) Explain how the capacitance is formed in the pn unction **(3marks)**

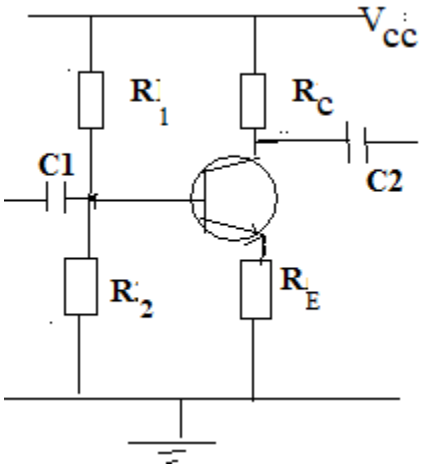

Figure Q2c

d) In the circuit of Figure Q2c, the transistor has the following h-parameters; h_{ie}=2kΩ h_{fe}=100 h_{oe}=5x10^{-5}S, $h_{\Re}$=0 Given the following bias components;R_1 = 50 kΩ
R_2 =20 kΩ R_C=5 kΩ R_E= 2kΩ C_E =100 µF, Vcc=9V, calculate for the stage;
i) the current gain ii) the voltage gain **(4 marks)**

e) Explain any THREE factors that affect the voltage gain at the high frequencies **(3marks)**

Question THREE

a) Draw the diagram of a light emitting diode and explain its operation **(7marks)**

b) Explain the operation of the circuit of Figure Q3b **(4marks)**

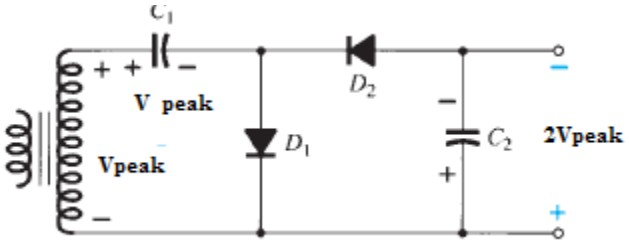

Figure Q3b

c) A half wave rectifier is connected to 240V 50 Hz supply via a step down transformer of turns ratio 20:1 to a load of 330 Ω. Neglecting the voltage drop across the diode ,calculate;

i) rms secondary voltage

ii) the peak secondary voltage

iii) the peak secondary current

iv) the average (dc) current flowing through the load . **(4 marks)**

d) A 5.6V,1W zener diode having a minimum current of 5mA is used in a shunt regulator to supply a load current of 20mA from a supply voltage which varies between 15V to 24 V, calculate;

i) a suitable value of the resistor and its power rating

ii) the power dissipated by the zener when the supply voltage is maximum

(5 marks)

Question FOUR

a) i) For the circuit of Figure 4a, V_{BE}= 0.7V, determine the operating point (I_{CQ},I_{BQ},V_{CEQ})

ii) Draw the dc load line

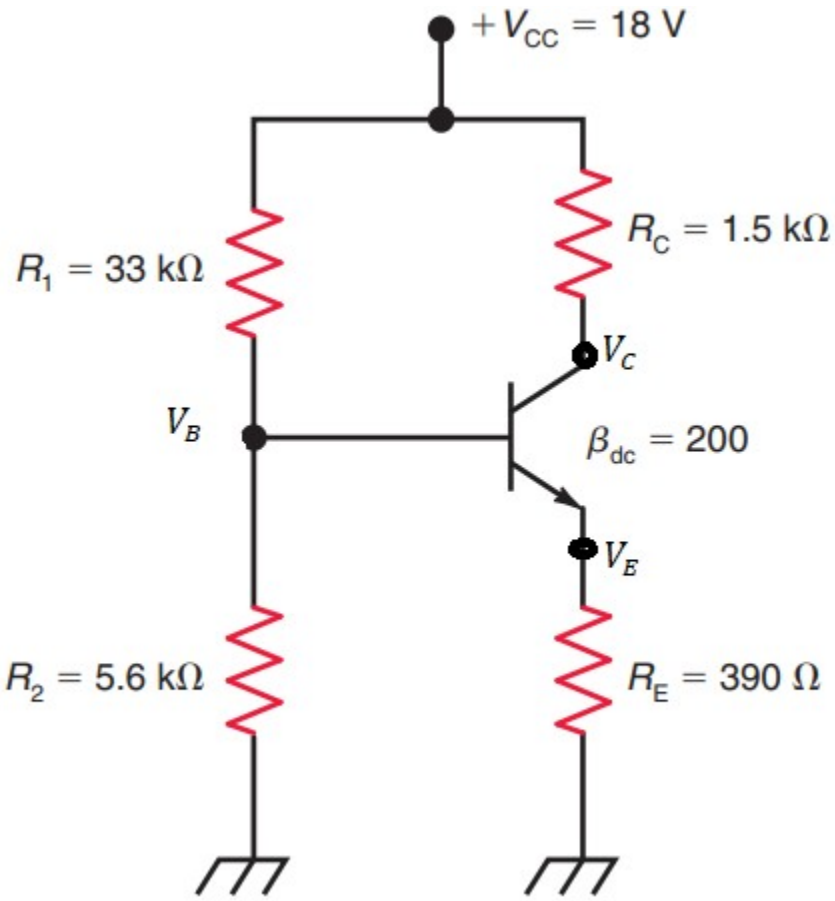

Figure 4a **(9 marks)**

b) A Multi stage amplifier consists of three identical stages such that R_C=2kΩ R_E= 1kΩ

R_1 = 27kΩ R_2=10kΩ C_E =100μ F. The transistor used has h_{fe}=150, h_{ie}=2kΩ.Determine the overall voltage gain of the circuit **(6marks)**

c) State any TWO features of each of the following transistor configurations

i) common collector ii) common base **(2 marks)**

c) Show that the common emitter dc current β is related to the dc current gain of common base α by the equation

$$\beta_{dc} = \frac{\alpha}{1-\alpha}$$ **(3 marks)**

Question FIVE

a) Define the following terms as applied to FETs;
i) transconductance ii) drain source resistance **(2marks)**

b) With the aid of construction diagram, explain the operation of n-channel depletion mosfet **(6marks)**

c) i) Draw the typical drain characteristics of n channel Junction FET and explain the distinct operating regions

ii) List any TWO properties of a FET that makes it ideal as electronic switch

iii) List any TWO advantages of FETs over BJTs **(8 marks)**

d) For the circuit of Figure Q5d **(4 marks)**

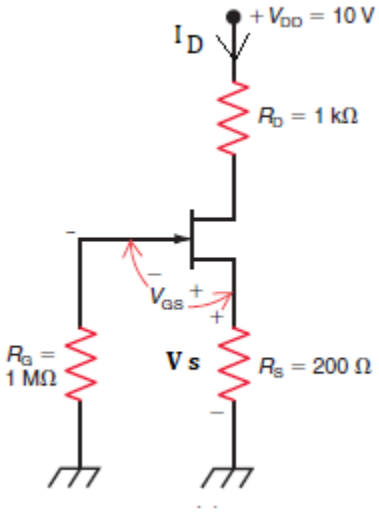

Figure Q5d