TECHNICAL UNIVERSITY OF MOMBASA
School of Engineering and Technology
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION 2024/2025

BACHELOR OF TECHNOLOGY IN ELECTRICAL AND ELECTRONIC ENGINEERING

TEE 4312: **DIGITAL SYSTEMS DESIGN**

TIME: 2 HOURS **SERIES:** April, 2025

INSTRUCTIONS TO CANDIDATES

1. You are required to have the following for this examination;
   - Answer Booklet
   - A non Programmable Calculator
2. This paper consists of **FIVE** Questions.
3. Answer **ANY THREE** Questions.

Question ONE

(a) (i) State the design procedures for a combinational logic circuit.

(ii) Using a 4 – to – 1 multiplexer, implement the function

$f(A, B, C, D) = \sum_m (1, 2, 4, 5, 9, 12, 13, 14)$ **(8 marks)**

(b) Design a logic circuit that has an enable input 'E' such that it converts a 3-bit Binary value to its equivalent Gray code when E = 1 and when E = 0, it converts a 3-bit Gray code to its Binary equivalent. Implement using Encoder and Decoder. **(12 marks)**

Question TWO

a) Explain the functions of the following digital devices:

(i) Binary comparator

(ii) Multiplexer

(iii) Logic analyser (**6 marks**)

b) With aid of a transition table, design a modulo-6 J-K flip-flop synchronous counter to repetitively count in the sequence 5, 4, 3, 2, 1, 0, 5 ….. Any illegal state will assume a value represented by 3 after a trigger pulse. (**14 marks)**

Question THREE

a) Obtain a minimum SOP expression for the function below using the abbreviated binary method of tabular minimization. (**10 marks**)

$$F(A,B,C,D,E) = \sum_m (3,4,7,9,11,12,15,16,18,19,20,23,24,26,27,28,31)$$

b) State the design procedures for a Finite State Machine. (**5 marks**)

c) Determine the size of the PROM required for implementing the following logic circuits:

i. a binary multiplier that multiplies two four-bit numbers;
ii. a dual 8-to-1 multiplexer with common selection inputs; (**5 marks**)

Question FOUR

a) Develop a full ADDER using NAND gates. (**10 marks**)

b) Derive the state table and state diagram of the sequential circuit shown in Figure Q4. (**10 marks**)

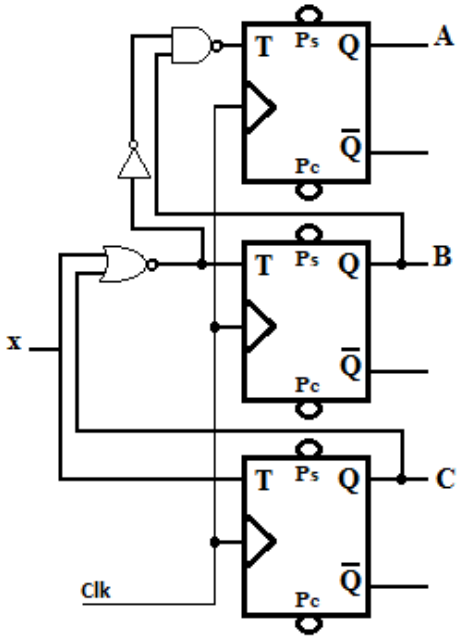

Figure Q4

Question FIVE

a) An electronic thermometer, designed for greenhouse use, has a 5-bit binary output representing a temperature range from 0^0C to 31^0C. A plug-in logic module is to be designed to output logic **1** when the temperature is even above 16^0C. Design NOR-to-NAND gate combinational network to implement this specification. (**10 marks**)

b) Obtain realizable logic diagram for a 4-to-2 priority encoder if the available signals are ~F_1[NL], F_0, ~I_2[NL], I_3, I_1, I_0. (**5 marks**)

c) Design a PLA device that implements a 3-bit odd parity generation. (**5 marks**)