



TECHNICAL UNIVERSITY OF MOMBASA

School of Engineering and Technology

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION 2024/2025

BACHELOR OF TECHNOLOGY IN ELECTRICAL AND ELECTRONIC ENGINEERING

TEE 4206 : DIGITAL ELECTRONICS I

TIME: 2 HOURS

SERIES: July, 2025

INSTRUCTIONS TO CANDIDATES

1. You are required to have the following for these examinations:
 - Answer Booklet
 - Non Programmable calculator
 2. This paper has **FIVE** Questions.
 3. Answer question **ONE** and any other **TWO** questions.
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Question ONE (COMPULSORY)

- a) Perform the following conversions:
 - i. $ACDF_{16}$ TO Octal
 - ii. 974.125_{10} to Binary **(4 marks)**
- b) Obtain results for the following arithmetic operations
 - i. $1010001_2 \div 1001_2$
 - ii. $55_{16} \times 2A_{16}$ **(6 marks)**
- c) Perform the following operations
 - i. $23_{16} - 76_{10}$ using 1's complement method
 - ii. $47_{10} - 25_{10}$ using 2's complement method
 - iii. $956_{10} + 46_{10}$ using 8421 BCD **(10 marks)**

Question TWO

- (a)
 - (i) State any **TWO** applications of Flip-flops
 - (ii) With the aid of a truth table and logic diagram explain the operation of a J-K flip-flop that uses NAND gates. **(11 marks)**
- (b) Design a **THREE** input combinational logic circuit that gives a High when the majority of the inputs are High. **(9 marks)**

Question THREE

- a) From Table 1 and using K-map minimization method,
- i) Write the minimized Boolean expression for output Z.
 - ii) Implement the circuit using minimal logic gates. **(8 marks)**

Table 1

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

- b) With the aid of a truth table and block diagram, explain the operation of a 4 – to – 1 channel multiplexer. **(6 marks)**
- (c) Obtain a Boolean expression for Exclusive NOR function and implement using basic gates. **(6 marks)**

Question FOUR

- (a) (i) Differentiate between synchronous and asynchronous binary counter
- (ii) Give ONE disadvantage of asynchronous counter. **(3 marks)**
- (b) Design a **THREE** input combinational logic circuit that gives a High when the majority of the inputs are High. **(9 marks)**

Question FIVE

- (a) State any **TWO**
- i) applications of flip flops
 - ii) modes of shift register operation. **(4 marks)**

(b) Obtain the results of the following operations in the respective base:

i $10101010_2 \div 100_2$

ii $44_8 \times 67_8$

(6 marks)

(c) With the aid of an enabled input 8 – to – 1 multiplexer IC implement the following switching expression.

$$f(A, B, C) = \sum_m(0, 2, 3, 4, 6)$$

(5 marks)

(d) Obtain truth table and Boolean expression of odd parity generation for 3-bit code. **(5 marks)**