TECHNICAL UNIVERSITY OF MOMBASA

School of Engineering and Technology

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
BACHELOR OF SCIENCE ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 4208 : DIGITAL ELECTRONICS I

TIME: 2 HOURS **SERIES:** July, 2025

INSTRUCTIONS TO CANDIDATES

1. You are required to have the following for this examination;
   - Answer Booklet
   - A non- Programmable Calculator
2. This paper consists of **FIVE** Questions.
3. Answer **Question ONE and ANY TWO other** Questions.

Question ONE (30 Marks) – (Compulsory)

(a) Define the following terms as used in digital electronics:
   (i) Code
   (ii) Radix **(2 Marks)**

(b) Perform the following operations:
   (i) 1101101 – 11001011 using 1's complement
   (ii) 258_{10} + 73_{10} using EX – 3 BCD **(4 Marks)**

(c) Perform the following conversions:
   (i) 349.75_{10} to binary
   (ii) 11111001001_2 to Hexadecimal **(4 Marks)**

(d) A computer operator types the following statement:
   GO TO 74
   Encode this information in ASCII format **(3 Marks)**

(e) Use the Boolean algebra to simplify the expression:

$$F = (A + \bar{B} + \bar{C}) \cdot (A + B + \bar{C})$$ **(4 Marks)**

(f) Implement the Exclusive OR function using NAND gates only. **(4 Marks)**

(g) Express the Boolean function $f(A,\ B,\ C) = (A+B)(\overline{B}+\overline{C})$ as:

(i) A product of maxterms

(ii) A sum of minterms **(6 Marks)**

(h) Show how a D flip-flop can be modified to perform like a T flip-flop. **(3 Marks)**

Question TWO

a) Explain the difference between the following terms:

i. Set up time and hold time

ii. Combination logic circuits and sequential circuits.

iii. Edge trigger and level trigger

iv. Mod-number and stage number **(8 Marks)**

b) i) The logic circuit in Figure Q2 is a register arrangement. Describe its operation by means of a characteristic table, assuming that register B is initially cleared and register A has the data 1101.

ii) Explain the operation performed by each register in (i) (**6 Marks**)

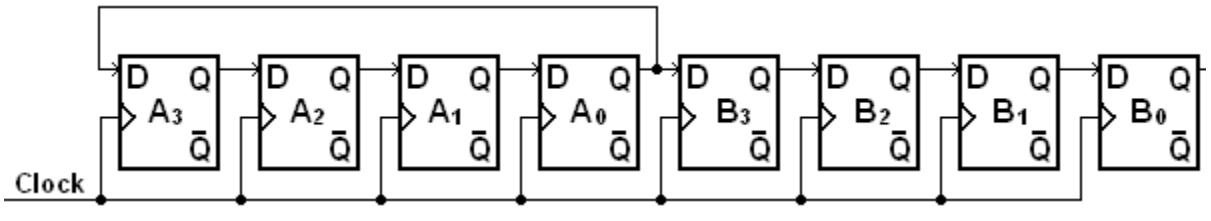

Figure Q2

(c) Given a 100MHz clock signal, derive a circuit using T flip-flops to generate a 50MHz and 25MHz clock signals. Draw the timing diagrams for all the three clock signals assuming negligible time delays. **(6 Marks)**

Question THREE

(a) (i) Explain why a de-multiplexer is referred to as 'data distributor'.

(ii) Sketch a block diagram of a 1- to – 4 de-multiplexer and obtain its truth table. **(5 Marks)**

(b) (i) Draw the truth table and develop the simplest circuit of a half adder.

(ii) Using blocks, show how two half adders can be used to realize a full adder. **(6 Marks)**

(c) (i) Obtain a truth table for a two 2-bit number comparator logic circuit that gives an output of logic 1 when the two numbers are equal.

(ii) Obtain the simplest expression for the comparator in (i).

(iii) Implement the two 2 – bit equality comparator using XOR gates and NOR gate. **(9 Marks)**

Question FOUR

(a) Explain the meaning of the following terms;

(i) Literal

(ii) Negative logic **(4 Marks)**

(b) Use the Venn diagrams to show that $(A+\overline{B}+\overline{C})(A+B+\overline{C}) = A+\overline{C}$ **(4 Marks)**

(c) The circuit in Figure Q4 implements the functions x and y. Re-design the circuit to implement the same functions with minimum number of NOR gates only.

(12 Marks)

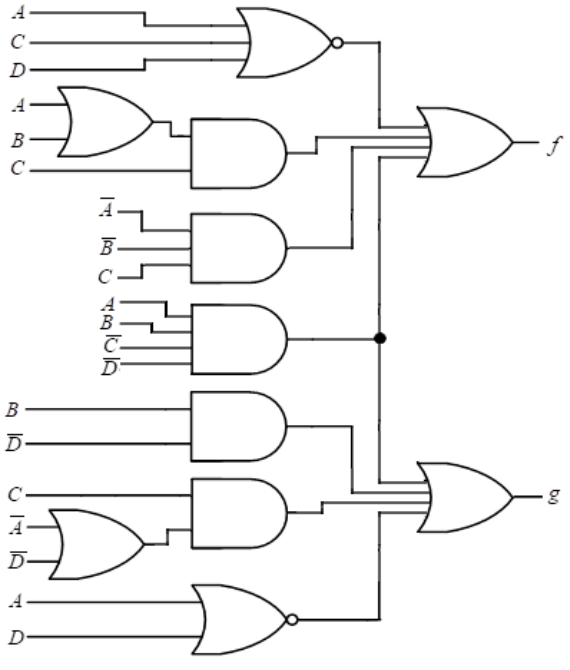

Figure Q4

Question FIVE

(a) Perform the following conversions:

(i) 89134_{10} to Octal

(ii) 10101011011 gray code to binary **(4 Marks)**

(b) Design the simplest sum-of-products logic circuit that implements the function $f(A,B,C) = \sum m(0,2,4,5,6)$ **(4 Marks)**

(c) A rocket launcher loaded onto a submarine is to be designed such that only three people; the Commander-in-charge and two Lieutenant Colonels can activate it to fire. It is desired that the rocket launcher fires only if the Commander-in-Charge and at least one Lieutenant Colonel give authorization. Design the simplest sum of products circuit that can be used for this purpose using basic gates. **(6 Marks)**

(d) (i) Use Boolean algebra to reduce the following expression:

$$x = \overline{A\overline{B} + ABC + A(C + A\overline{C})}$$

(ii) Use a truth table to prove that $AC + A\overline{C} + \overline{A}BC = A + BC$ **(6 Marks)**

The 7 bit ASCII code

Bit Positions 3210	**Bit Positions** 654							
	000(0)	001(1)	010(2)	011(3)	100(4)	101(5)	110(6)	111(7)
0000(0)	NUL	DLE	SP	0	@	P	'	p
0001(1)	SOH	DC_1	!	1	A	Q	a	q
0010(2)	STX	DC_2	″	2	B	R	b	r
0011(3)	ETX	DC_3	#	3	C	S	c	s
0100(4)	EOT	DC_4	$	4	D	T	d	t
0101(5)	ENQ	NAK	%	5	E	U	e	u
0110)6)	ACK	SYN	&	6	F	V	f	v
0111(7)	BEL	ETB	′	7	G	W	g	w
1000(8)	BS	CAN	(	8	H	X	h	x
1001(9)	HT	EM	)	9	I	Y	i	y
1010(A)	LF	SUB	*	:	J	Z	j	z
1011(B)	VT	ESC	+	;	K	[	k	{
1100(C)	FF	FS	,	<	L	\	l	|
1101(D)	CR	GS	-	=	M	]	m	}
1110(E)	SO	RS	.	>	N	^	n	~
1111(F)	SI	US	/	?	O	–	o	DEL

Definition of Abbreviations

NUL	Null/Idle	SI	Shift in
SOH	Start of header	DLE	Data link escape
STX	Start of text	DC1-DC4	Device control
ETX	End of text	NAK	Negative acknowledgement
OET	End of transmission	SYN	Synchronous idle
ENQ	Enquiry	ETB	End of transmission block
ACK	Acknowledgement	CAN	Cancel (error in data)
BEL	Audible signal	EM	End of medium
BS	Backspace	SUB	Special sequence
HT	Horizontal tab	ESC	Escape
LF	Line feed	FS	File separator
VT	Vertical tab	GS	Group separator
FF	Form feed	RS	Record separator
CR	Carriage return	US	Unit separator
SO	Shift out	DEL	Delete/Idle