TECHNICAL UNIVERSITY OF MOMBASA

FACULTY OF ENGINEERING AND TECHNOLOGY

ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT

UNIVERSITY EXAMINATION FOR:

DIPLOMA IN ELECTRICAL & ELECTRONIC ENGINEERING

EEE 2202: DIGITAL ELECTRONICS II.

END OF SEMESTER EXAMINATION

SERIES: AUGUST, 2024

TIME: 2HOURS

DATE: Pick Date Select Month Pick Year

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of FIVE questions. Attempt any THREE.

Do not write on the question paper.

Question ONE

a) Differentiate between Decoders and encoder **(4marks)**

b) Explain the term priority binary encoder. **(2marks)**

c) Design a data handling circuit that can be used to relay various projects results of four classes to an exam coordinator . Available data: one channel, Telecommunication class code, Power group class code, instrumentation group code, Automation group class code and basic gates .Use the truth table to explain the operation of the designed circuit mentioning how the outputs would be realized. **(6marks)**

d) State any three applications of Demultiplexers **(3marks)**

e) Design and implement a 3-line to 8-line decoder **(5marks)**

Question TWO

a) With the aid of a diagram explain the operation of a successive approximation ADC **(5marks)**

b) Assume the following values for the ADC clock frequency = 1 MHz; VT = 0.1 mV; DAC has F.S. output = 10.23 V and a 10-bit input. Determine the following values.

a. The digital equivalent obtained for VA = 3.728 V.
b. The conversion time.
c. The resolution of this converter. **(5marks)**

c) Explain the advantages of R/2R ladder DACs over that of Binary weighted resistor. **(4marks)**

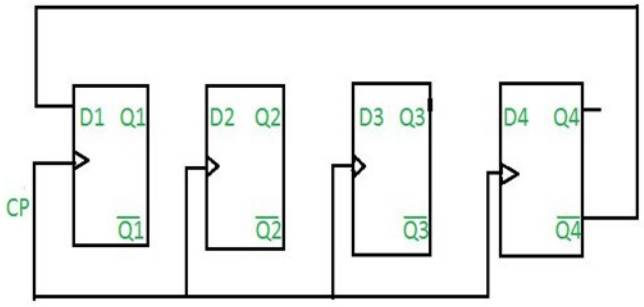
d) Explain the following terms

i. Step size
ii. Conversion time **(2marks)**

e) Explain the function of the comparator in ADC hence state the major disadvantage of the digital ramp type ADC. **(4marks)**

Question THREE

a) with the aid of a block diagram and timing diagrams **d**esign a synchronous MOD-5 counter . (6marks)
b) Outline any two differences between the edge triggering and level triggering .(3marks)
c) With the aid of a diagram explain the operation of a 4 bit binary SIPO shift register using D- type flip-flops. (6marks)
d) The circuit of fig. 2 is a 4-bit Johnson counter, using the truth table, Determine the total number of used and unused states in the counter. (5marks)



Question Four

a) Explain the following terms (i) access time (ii) cycle time of a memory (4marks)
b) Differentiate between Dynamic RAM and static RAM (4marks)
c) Draw the structure of a static RAM cell Using 6 FETs and explain its operation. (5marks)
d) Describe any TwO types of ROMs (4marks)
e) Draw the truth table for the circuit shown in fig. (3marks)

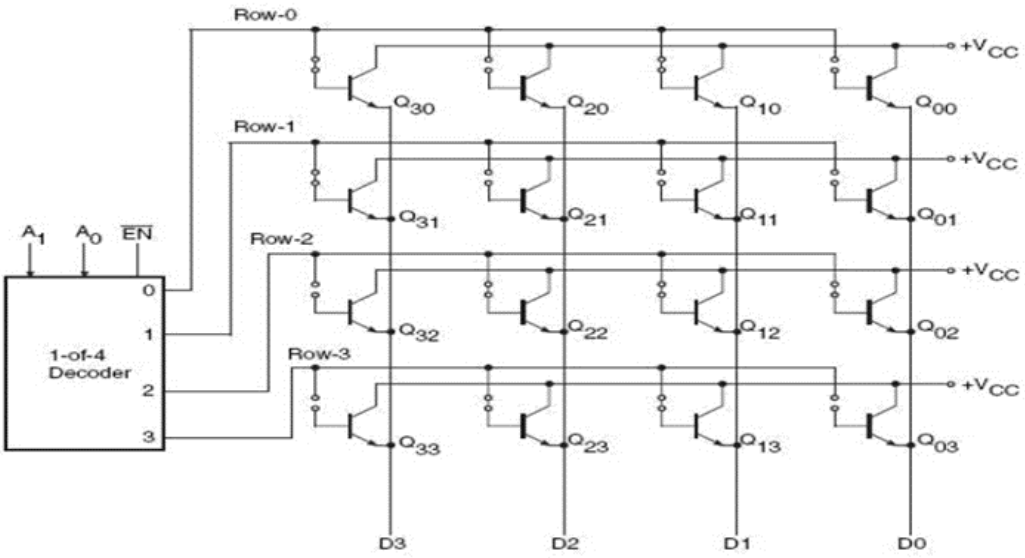


Fig. 2

Question FIVE

a) With the aid of diagrams explain the following terms highlighting any differences between them
   i. Combinational
   ii. Sequential (4marks)

b) With the aid of a logic circuit and timing diagram explain the operation of a clocked J-K flip-flop

(6marks)

c) Explain how race condition occurs in JK flipflops hence use a diagram to show how it can be eliminated (10marks)