TECHNICAL UNIVERSITY OF MOMBASA

INSTITUTE OF COMPUTING AND INFORMATICS

DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY

UNIVERSITY EXAMINATION FOR:

BACHELOR OF TECHNOLOGY IN ICT AND

BACHELOR OF TECHNOLOGY & APPLIED PHYSICS

EIT 4304: COMPUTER ARCHITECTURE AND ORGNIZATION/
EIT 4309: COMPUTER ORGNIZATION AND ARCHITECTURE

SPECIAL/SUPPLEMENTARY EXAMINATION

SERIES: SEPTEMBER 2018

TIME: 2HOURS

DATE: Sep 2018

Instructions to Candidates

You should have the following for this examination
-Answer Booklet, examination pass and student ID
This paper consists of **FIVE** questions. Attemptquestion ONE (Compulsory) and any other TWO questions.
Do not write on the question paper.

QUESATION ONE (30 MARKS)

A. Using relevant examples discuss the following operations of a microprocessor

i. Fetch Cycle [5 marks]
ii. Execution Cycle [5 marks]

B. There are different ways to classify computers. One of the more widely used classifications, in use since 1966, is called Flynn's Taxonomy. Using relevant examples and with aid of diagram discuss the following classification of computers

i. SISD Computer Architecture [5 marks]
ii. SIMD Computer Architecture [5 marks]
iii. MISD Computer Architecture [5 marks]
iv. MIMD Computer Architecture [5 marks]

QUESATION TWO (20 MARKS)

As a hardware designer consultant for HP, you are required to design a direct mapping cache scheme of set size 4 blocks with the following memory cache parameters:

a. Memory Size = 528KB
b. Cache Size = 256 KB
c. Block Size 8B

Calculate the number the following address bit partitioning

i. Offset bit [3 marks]
ii. Index bit [7 marks]
iii. Tag bit [3 marks]
iv. Draw the design diagram for the Address Bit Partitioning [7 marks]

QUESATION THREE (20 MARKS)

Different microprocessor architecture support various data size. Instruction set can be processes in various data size. Using relevant examples and with the aid of diagram, discuss the following data sizes

i. Nibble [5 marks]
ii. Byte [5 marks]
iii. Word [5 marks]
iv. Long word [5 marks]

QUESATION FOUR (20 MARKS)

The average memory access time for a microprocessor with 1 level of cache is 2.4 clock cycles.

- If data is present and valid in the cache, it can be found in 1 clock cycle.
- If data is not found in the cache, 80 clock cycles are needed to get it from off-chip memory

Designers are trying to improve the average memory access time to obtain a 65% improvement in average memory access time, and are considering adding a 2nd level of cache on-chip.

- This second level of cache could be accessed in 6 clock cycles
- The addition of this cache does not affect the first level cache's access patterns or hit times
- Off-chip accesses would still require 80 additional CCs.

Calculate the following

i. Miss Rate [5 marks]
ii. Hit Rate [5 marks]
iii. Speedup [5 marks]
iv. How often must data be found in the 2nd level cache? [5 marks]

QUESATION FIVE (20 MARKS)

A. A bus is shared communication link. It has a single set of wires used to connect multiple subsystems. Give two advantages and two disadvantages of buses. [5 marks]

B. Buses are traditionally classified as one of 3 types. Discuss the following classification of buses.

i. Processor memory buses [5 marks]
ii. I/O buses [5 marks]
iii. Backplane buses [5 marks]