

TECHNICAL UNIVERSITY OF MOMBASA

FACULTY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF MEDICAL ENGINEERING

UNIVERSITY EXAMINATION FOR:

DIPLOMA IN MEDICAL ENGINEERING

EHL 2204: DIGITAL ELECTRONICS

END OF SEMESTER EXAMINATION

SERIES: AUGUST 2019

TIME: 2 HOURS

DATE: Pick Date Aug 2019

Instructions to Candidates

You should have the following for this examination

-Scientific calculator

This paper consists of FIVE questions. Attempt any THREE questions. Do not write on the question paper.

QUESTION ONE

a)

i) Convert 1001010100.00112 to Octal ii) Perform 19-8 by 2 's complement iii) Minimize the following equation using k-maps and hence implement using NAND gates only

$$y = A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C\bar{D}$$

(9 marks)

b)

i) Discuss the advantages of edge triggering compared to level triggering

ii) Draw the general TTL IC pin layout iii) Design and implement a MOD-5 ripple up counter

(11 marks)

QUESTION TWO

a)

i) Convert AF16 to binary ii) Explain what is meant by forbidden numbers in BCD iii) Simplify $(\bar{B} + \bar{B}C)(\bar{B} + \bar{B}C)(\bar{B} + D)$

(8 marks)

b)

i) Using suitable diagrams, explain the operation of a PGT edge detector ii) Design an excess-3-to-BCD code-converter using minimum number of gates

(12 marks)

QUESTION THREE

a)

i) Convert 325810 to hexadecimal ii) State any TWO applications of BCD code iii) Explain the two broad logic families classification

(8 marks)

b) Design, using the minimum number of logic gates, an electronic circuit to replace an interlock system in a certain dialysis machine controlled by sensors A, B, C and D. Switch (S) should put ON the machine, EXCEPT when;

- i) A is HIGH and C is LOW, or
- ii) B is LOW and D is HIGH, or
- iii) B is HIGH and D is LOW, or
- iv) A is LOW and C is HIGH

(12 marks)

QUESTION FOUR

a)

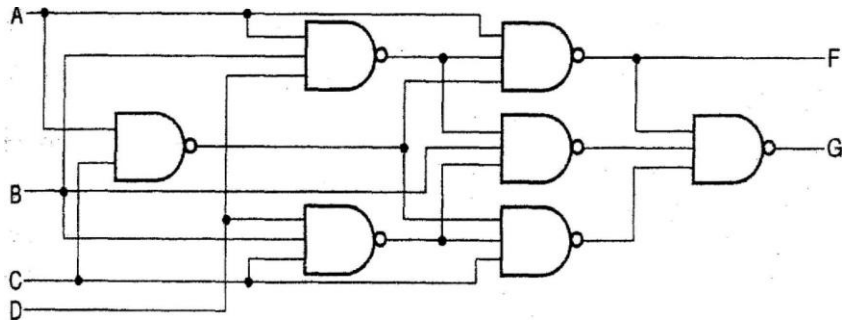
i) Draw the general CMOS IC pin layout ii) Dec 2435-9786 by 10's complement iii) Explain how Gray-code can reduce chances of error in electronic circuits

(7 marks)

b) Design a FULL ADDER using NAND gates ONLY

c) Find the simplified Boolean functions for outputs F and G of the circuit in the following figure

(13 marks)



QUESTION FIVE

a)

i) Perform 1-7 by 1's complement 3 ii) Design a parity generator to generate an Even parity bit for a 4-bit word using NOR gates only.

(9 marks)

b)

i) Design a HALF SUBTRACTOR using NAND gates ONLY ii) List FOUR Logic families

(1 I Marks)