TECHNICAL UNIVERSITY OF MOMBASA

FACULTY OF APPLIED & HEALTH SCIENCES

DEPARTMENT OF MATHEMATICS & PHYSICS

UNIVERSITY EXAMINATION 2017/2018

BACHELOR OF SCIENCE IN STATISTICS & COMPUTER SCIENCE

EEE 4350: DIGITAL ELECTRONICS AND DEVICES

SPECIAL/SUPPLEMENTARY EXAMINATION

SERIES: SEPTEMBER 2018

TIME: 2 HOURS

DATE: SEPTEMBER 2018

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of FIVE questions. Attempt **Question ONE (Compulsory)** and any other **TWO Questions**

Do not write on the question paper.

QUESTION 1

(a) Differentiate between combinational and sequential logic circuits and give two examples of each. **(4 marks)**

(b) Describe the following terms with respect to logic gates

(i) Fan-in

(ii) Propagation delay time

(iii) Fan-out

(6 marks)

(c) State FOUR advantages of digital systems over analogue ones. **(4 marks)**

(d) A logic function is given by: $f(A, B)=\sum 2,3$ Show that $f(A, B)=\prod 0, 1$ **(6 marks)**

(e) Describe a Half-adder and with the help of a suitable truth table, implement its logic circuit. Explain how a Full-adder can be implemented from a half-adder. **(10 marks)**

QUESTION 2

(a) Describe with help of suitable block diagrams the subtraction of two 4-bit binary numbers using Full-subtractors.

(6 marks)

(b) Define a decoder. With the help of a Truth table implement a 2-to-4 decoder.

(8 marks)

(c) Simplify using Boolean algebra, the following logic expression:

$$F = C + \overline{BA} + \overline{B + A} + C$$

(6 marks)

QUESTION 3

(a) (i) Define a shift register.
(ii) Describe with the help of suitable diagrams the construction and operation of a SIPO Shift register.

(10 marks)

(b) State De-Morgan's theorem. **(4 marks)**

(c) Using Karnaugh mapping, simplify the following logic expressions:

$$F = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,CD + \overline{A}\,B\,\overline{C}\,D + \overline{A}\,BC + \overline{A}\,BCD + AB\,\overline{C}$$

(6 marks)

QUESTION 4

(a) Define a de-multiplexer. With the help of a suitable logic circuit describe the operation of 1-to-4 de-multiplexer.

(12 marks)

(b) Illustrate how 3-input AND gate can be implemented using NAND gates only.

(6 marks)

(c) A logic expression is given by $f(A, B, C) = \prod 1, 3, 8$. Express the logic expression as *Sum of products* of the three logic variables A, B and C. **(2 marks)**

QUESTION 5

(a) Describe FIVE major design procedures (in logical order) for combinational logic circuits.

(10 marks)

(b) Using J-K flip flops:
(i) Draw the logic circuit of a 2-bit Asynchronous *up-counter* using J-K flip-flops.

(ii) Sketch timing diagrams at the respective output Q_A and Q_B for up to 4 clock pulses given that the output from Q_A is the least significant bit and that from Q_B the most significant bit. Assume initially $Q_A=Q_B=1$.

(iii) Draw the truth table for the counter (up to 4 clock pulses)

(8 marks)

(c) State how the counter in (b) can be converted to an Asynchronous *down-counter*.

(2 marks)