TECHNICAL UNIVERSITY OF MOMBASA

Faculty of Engineering and Technology

Department of Medical Engineering

UNIVERSITY EXAMINATION FOR:

Bachelor of Science in Medical Engineering

EEE 4330 Digital Electronics I

SPECIAL/SUPPLEMENTARY EXAMINATION

SERIES: SEPTEMBER 2018

TIME: 2 HOURS

DATE: SEP 2018

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **five** Questions; Question ONE is compulsory. In addition attempt any Other TWO Questions.

Do not write on the question paper.

Question ONE.

a) Perform the following:

i. Number conversions
   I. $ACD3_{16}$ to Octal
   II. 974.125_{10} to Binary

ii. Arithmetic operations
   i. $1100_2 \div 101_2$
   ii. $1011_2 + 110_2$

iii. Perform the following arithmetic operations
   i. $17_{10} - 31_{10}$ using 2's Complement
   ii. $13_{10} - 9_{10}$ using 1's Complement

12 marks

b) For the following switching function

$$F = \overline{A.\overline{B} + \overline{A}.C}$$

i. Draw its combinational logic circuit

ii. Derive its truth table

iii. Implement it using an appropriate decoder 8 marks

c.) Implement a minimized four input combinational logic circuit that produces a logic '1' at the output when at least TWO inputs are at logic '1'

10 marks

Question TWO.

a.) Explain the function of the following combinational logic devices

i. Encoder
ii. Comparator
iii. Multiplexer
iv. Decoder
v. Demultiplexer 10 marks

b.) With aid of a truth table design a minimized combinational logic circuit of a half adder

10 marks

Question THREE

a.) i. State any TWO applications of Flip-flops

ii. With the aid of a truth table and logic diagram explain the operation of each the FOUR types of Flip-flop 12 marks

b.) Implement a minimized combinational logic circuit that effects the following Boolean function

$F_{(A,B,C,D)} = \Sigma_m (1,3,5,7,9,11,13,15)$ 8 marks

Question FOUR

a.) Differentiate between

i. synchronous and asynchronous binary counter
ii. negative and positive edge triggered flip-flop

8 marks

b.) With aid of timing diagrams and JK flip-flops explain the operation of a 3-bit ripple counter

12 marks

Question FIVE

a.) With the aid of block diagram outline the four modes of shift register operation 4 marks

b.) Design a 4-bit ring counter using D flip flops and give its ONE advantage and ONE disadvantage. 6 marks

c.) i Using an 8 – to – 1 multiplexer implement the following switching function

$$F_{(A, B, C)} = \Sigma_M (0, 2, 4, 6)$$

ii. Using a 4- to – 2 decoder implement a Half adder circuit. 10 marks