TECHNICAL UNIVERSITY OF MOMBASA

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION 2016/2017

UNIVERSITY EXAMINATIONS FOR THE DEGREE OF BACHELOR OF ELECTRICAL AND ELECTRONIC ENGINEERING (BSEE)

EEE 2518 : DIGITAL SYSTEMS DESIGN I

TIME: 2 HOURS **SERIES:** SEPTEMBER, 2018

INSTRUCTIONS TO CANDIDATES

1. You are required to have the following for this examination;
   - Answer Booklet
   - A non Programmable Calculator
2. This paper consists of **FIVE** Questions.
3. Answer **Question ONE** and any other **TWO** Questions.
4. **This paper consists of THREE printed pages.**

Question ONE

a) Obtain realizable logic diagram for a 4-to-2 priority encoder for the following available signals ~F_1[NL], F_0, ~I_2[NL], I_3, I_1, I_0. Also implement it using minimum number of one type of gates. (**8 marks**)

b) With aid of a transition table, design a modulo-5 D flip-flop based synchronous counter to repetitively count in the sequence 0, 1, 2, 3, 5, 0, 1 …. The unused states will assume a value represented by 3. Other than the flip-flop IC packages, use optimal IC packages. (**12 marks)**

c) With aid of a truth table, develop full adder logic and implement using 4-to-1 multiplexers with minimum external circuitry. (**10 marks**)

Question TWO

a) (i) State the design procedures for a sequential logic circuit.
(ii) Using a 4 – to – 1 multiplexer, implement the function
$f(A,B,C,D) = \sum_m (0, 2, 4, 5, 6. 8, 10, 11, 12, 15)$ **(7 marks)**

b) Given the state diagram of Figure Q2, generate the state table and design a sequential circuit using D-flip flops. (**13 marks**)

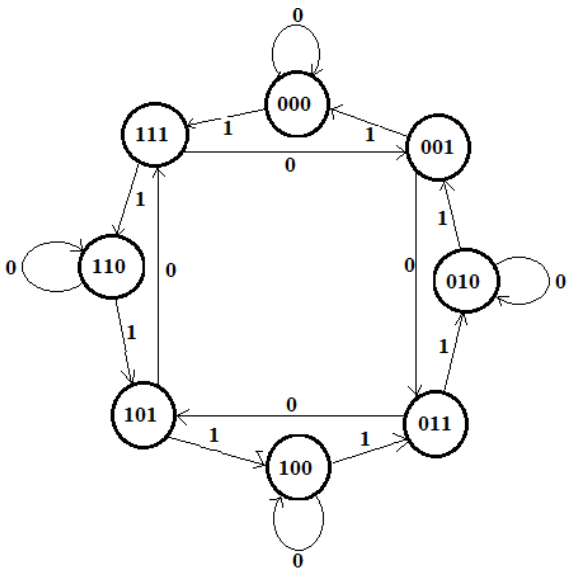

Figure Q2

Question THREE

a) Explain the functions of the following digital devices:

(i) Multiplexer
(ii) Binary comparator
(iii) Encoder (**6 marks**)

b) A certain building has a central heating system controlled by five thermostats in various locations. Each thermostat has a logic **1** output for too low a temperature, and logic **0** for too high temperature (thermostat cut off). Design NOR-to-NOR gate combinational networks to implement this specification. (**8 marks**)

c) Realize a half adder using NAND gates only. (**6 marks**)

Question FOUR

a) Using the tabular method minimization technique, obtain a minimum SOP expression for the function F (A, B, C, D, E) = $\sum_m$ = (2, 5, 6, 8, 9, 10, 11, 12, 13, 15, 16, 17, 18, 19, 20, 25, 26, 27, 29, 31) **(9 marks)**

b) Design a logic circuit that has an enable input 'E' such that it converts a 3-bit binary value to its equivalent 3-bit gray code when E = 0 and when E = 1, it converts a 3-bit gray code to its binary equivalent. Implement using appropriate decoder and encoder with minimum external IC package. **(11 marks)**

Question FIVE

a) Given two 2-bit binary numbers A and B, design a PLA device to implement a magnitude comparator to produce outputs for A being 'equal to', 'less than' and 'greater than' B. (**14 marks**)

b) Determine the size of the PROM required for implementing the following logic circuits:
   i. a binary multiplier that multiplies two four-bit numbers;
   ii. a dual 8-to-1 multiplexer with common select inputs;
   iii. a single-digit BCD adder/subtractor with a control input for selection of operation.

(**6 marks**)