TECHNICAL UNIVERSITY OF MOMBASA

FACULTY OF ENGINEERING & TECHNOLOGY

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION 2017/2018

THIRD YEAR FIRST SEMESTER EXAMINATION FOR THE

DEGREE OF BACHELOR OF SCIENCE (ELECTRICAL & ELECTRONIC ENGINEERING)

EEE 2305: DIGITAL ELECTRONICS I

SPECIAL/SUPPLEMENTARY EXAMINATION

SERIES: SEPTEMBER 2018

TIME: 2 HOURS

DATE: SEPTEMBER 2018

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of FIVE questions. Attempt **Question ONE (Compulsory)** and any other **TWO Questions**

Do not write on the question paper.

Question ONE

a. Differentiate between synchronous and asynchronous sequential circuits (6 marks)

b. De-Morganize the Boolean expression below and implement the simplified expression using a minimum number of NAND gates.

$$Y = \overline{\left(\overline{A \cdot B} + \overline{C}\right) \cdot \left(\overline{A} + \overline{B \cdot C}\right)}$$ (8 marks)

c. With the aid of a block diagram, XOR implementation and truth table describe the operation of a full-adder. (8 marks)

d. In a 4-stage ripple counter, the propagation delay of a Flip-flop is 50 ns. If the pulse width of the strobe is 30 ns, find the maximum frequency at which the counter operates reliably. (2 marks)

e. Perform the following operations:

i. $3F_{16}$ - $5C_{16}$ (using 2's complement)

ii. 36_{10} + 63_{10} (using Excess-3 code)

iii. 11111_2 –$F.F_{16}$ (using the Hexadecimal subtraction)

(6 marks)

Question TWO

a. Show that $A.(B \oplus C) = A.B \oplus A.C$ (5 marks)

b. Use a Karnaugh Map to simplify the following Boolean expression:

$$F(w,x,y,z) = \sum m(1,3,7,11,15)$$

that has the don't care conditions

$$d(w,x,y,z) = \sum m(0,2,5)$$ (5 marks)

c. Show the states of a 4-bit SISO register for data input 1101 using a block diagram, waveforms and transition table. Assume the registers contain ones initially. Use positive-edge triggered D-flip-flops (10 marks)

Question THREE

a. Define the term race around as used in flip-flops. (2 marks)

b. In the flip-flop circuit of **Figure Q3.1** show that if:

i. $P_r = 0 \; and \; C_r = 1, then \; Q = 1$ (independent of *S*, *R*, and *CK)*

ii. $P_r = 1 \; and \; C_r = 0, then \; Q = 0$ (independent of *S*, *R*, and *CK)*

iii. $P_r = C_r = 1,$ then it functions as a clocked SR flip-flop (10 marks)

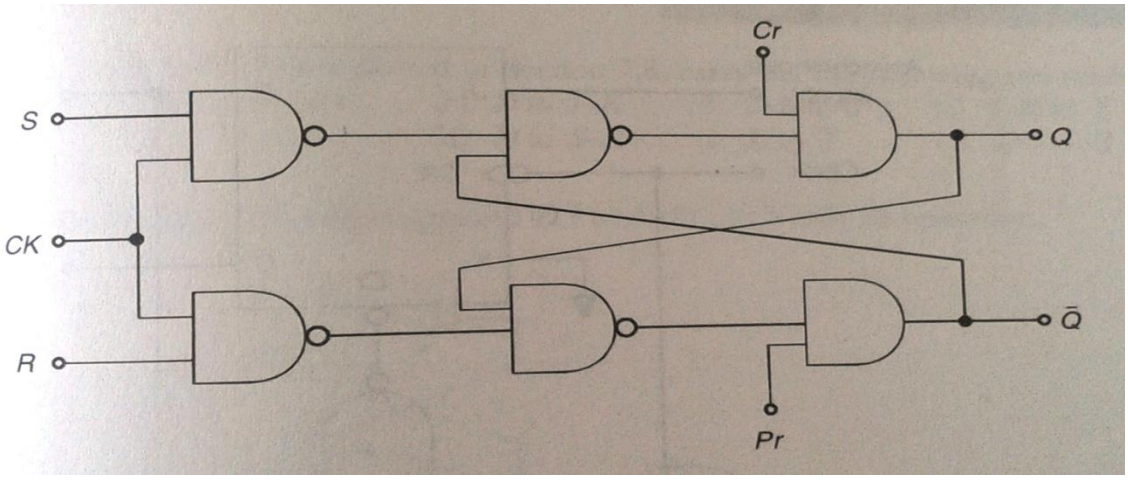

Figure Q3.1

c. **Figure Q3.2** shows a positive edge-triggered D-type flip-flop. Verify its operation. (8 marks)

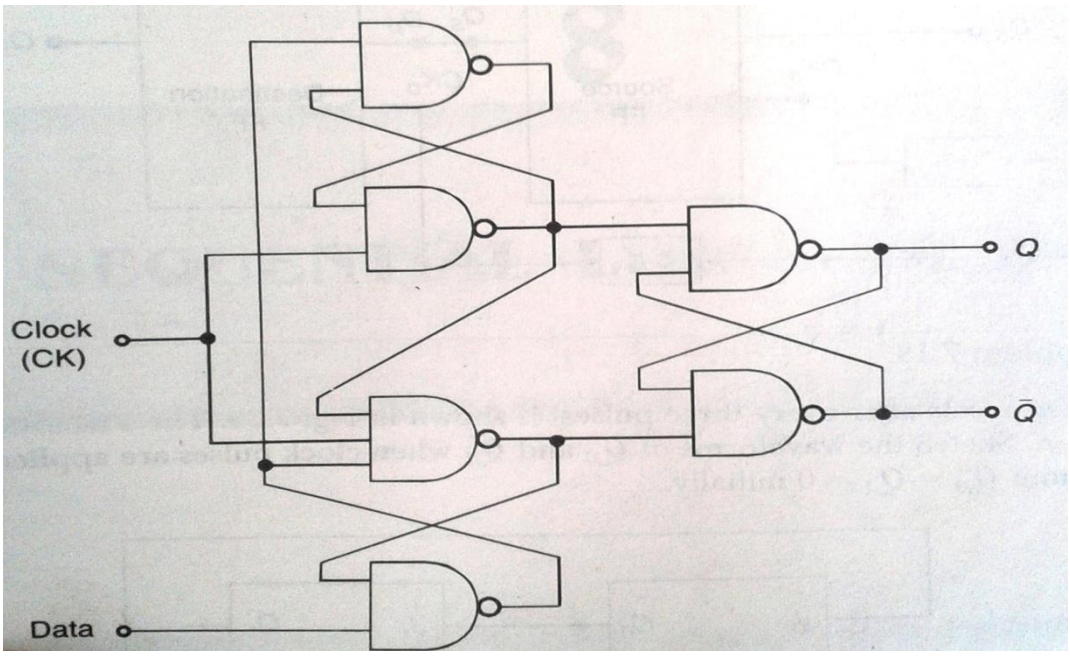

Figure Q3.2

Question FOUR

a. Design (without minimizing), a logic circuit using NOR gates only with three input variables that will produce a 1 output when any two input variables are 1's. (6 marks)

b. Design a J-K counter that endlessly goes through states 2, 4, 5, 7, 2, 4…… (14 marks)

Question FIVE

a. Tyrone Shoelaces has invested a huge amount of money into the stock market and doesn't trust just anyone to give him buying and selling information. Before he will buy a certain stock, he must get input from three sources. His first source is Pain Webster, a famous stock broker. His second source is Meg A. Cash, a self-made millionaire in the stock market, and his third source is Madame LaZora, a world-famous psychic. After several months of receiving advice from all three, he has come to the following conclusions:

- Buy if Pain and Meg both say yes and the psychic says no.
- Buy if the psychic says yes.
- Don't buy otherwise.

Construct a truth table and find the minimized Boolean function to implement the logic telling Tyrone when to buy. Implement the minimized Boolean function. (6 marks)

a. i. Obtain the truth table for the logic circuit shown in **Figure Q5**

ii. Design the circuit in (i) using minimum number of NOR gates (14 marks)

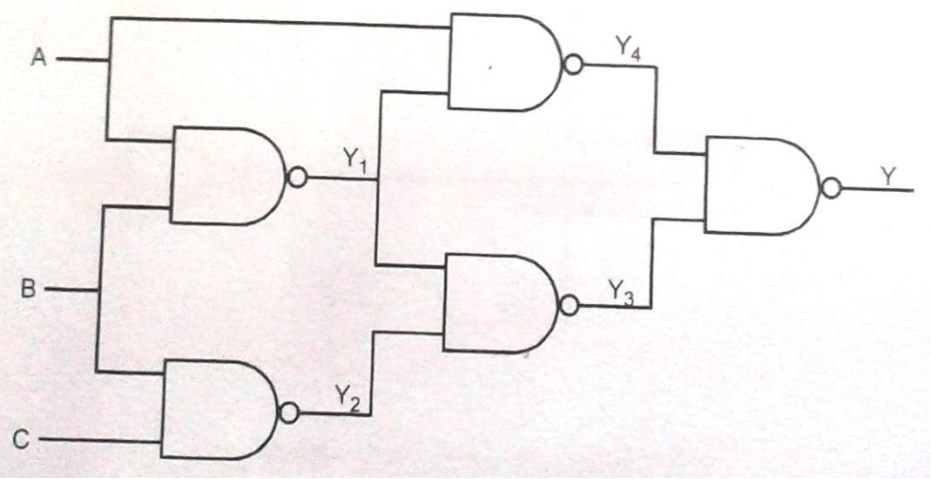

Figure Q5