TECHNICAL UNIVERSITY OF MOMBASA

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING
UNIVERSITY EXAMINATIONS FOR DIPLOMA IN TECHNOLOGY (ELECTRICAL & ELECTRONIC ENGINEERING)

EEE 1103

DIGITAL ELECTRONICS II

END OF SEMESTER EXAMINATION

SERIES: AUGUST 2019

TIME: 2 HOURS

Instructions to Candidates

You should have the following for this examination
-Answer Booklet, examination pass and student ID
This paper consists of **five** Questions
Attempt any THREE Questions.
Do not write on the question paper.

QUESTION ONE

a) Define the following terms as applied to logic families ;

i) noise immunity ii) fan out (2 marks)

b) i) Explain the operation of figure 1

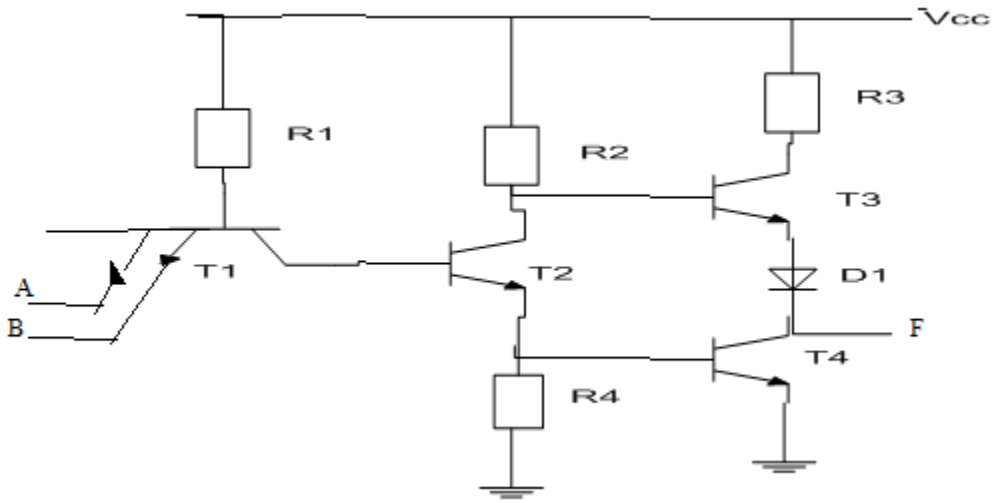


Figure 1

. ii) State any TWO advantages of totem pole output over the open collector

iii) State any TWO advantage and any ONE disadvantage of CMOS gates over their TTL counterparts (10 marks)

c) Draw the diagram of CMOS transmission gate and explain its operation (5 marks)

d) A unit load (uL) for a logic family is as follows;

1uL = 50µA HIGH state and

=2.5mA LOW state

If HIGH state output current I_{OH} =400 µA and LOW state output current I_{OL} =17.5mA Determine the fan out of the gate (3 marks)

QUESTION TWO

a) Describe the following types of multivibrators

i) astable ii) bistable (4 marks)

b) Explain the operation of the circuit of figure 2

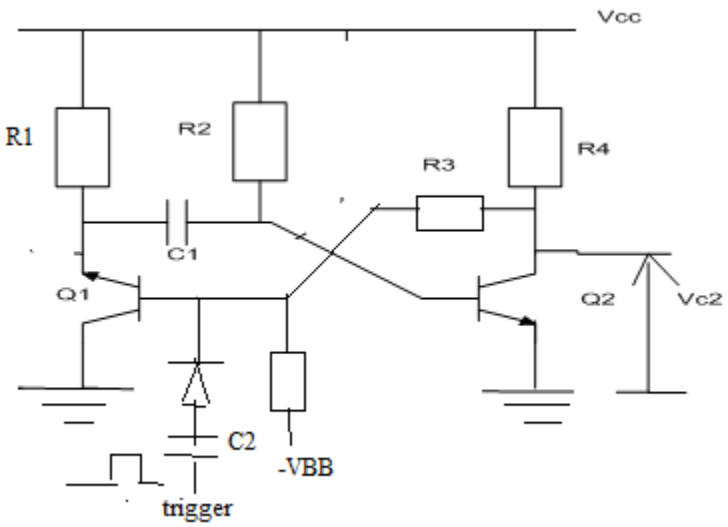


Figure 2 (6 marks)

c) An astable multi-vibrator has the following components;

C1=22nF C2=10nF R2=4.7k R1=10k, Calculate;

i) pulse repetition frequency ii) duty cycle (6 marks)

d) i) State any TWO applications of a mono stable multivibrators

ii) Explain any TWO advantages of 555 timers over the discrete type multivibrators.

4 marks)

QUESTION THREE

a) i) Draw the logic circuit ,and truth table of a J-K flip-flop

ii) Explain the advantage of J-K Flip Flop over the R-S flip flop

iii) The following waveforms figure 3 are applied to the leading edge triggered JK Flip Flop. Draw the resulting waveform at Q and $\overline{Q}$ if the Flip flop is initially RESET (8marks)

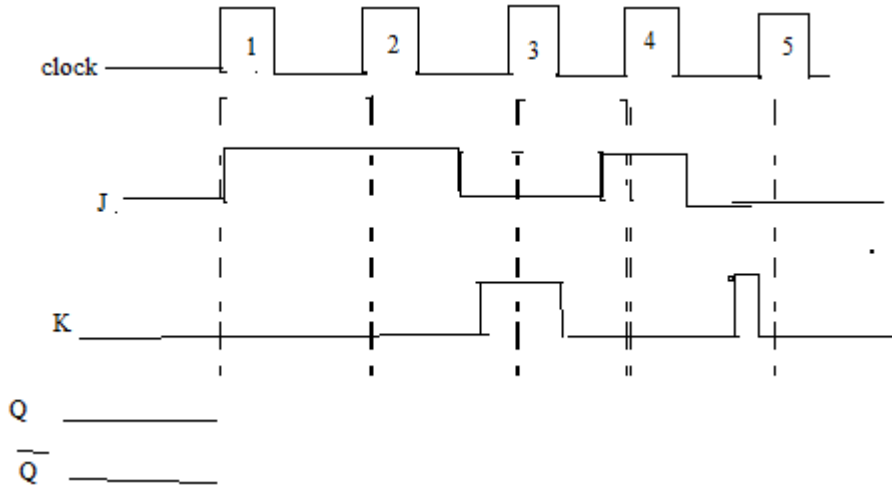


Figure 3

b) i) Explain the operation of figure 4 assume initially Q=0 and draw the output waveform

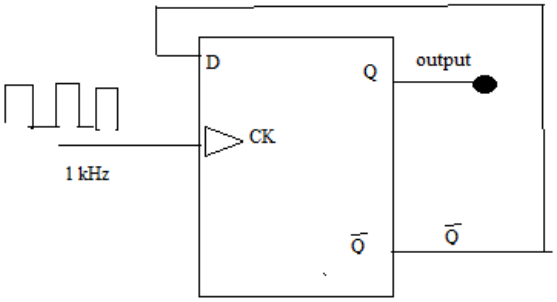


Figure 4

ii) Draw the timing diagrams for a NOR gate RS Flip Flop if the SET and RESET inputs go HIGH for 0.1ms at the following terms;

SET: 1 ms, 4ms, 5.5ms, 7ms

RESET: 2ms, 3ms,5ms,8ms

Assume initially Q is LOW and $\overline{Q}$ is HIGH (9 marks)

c) Distinguish between synchronous and asynchronous inputs of a flip flop and give an example of each (3 marks)

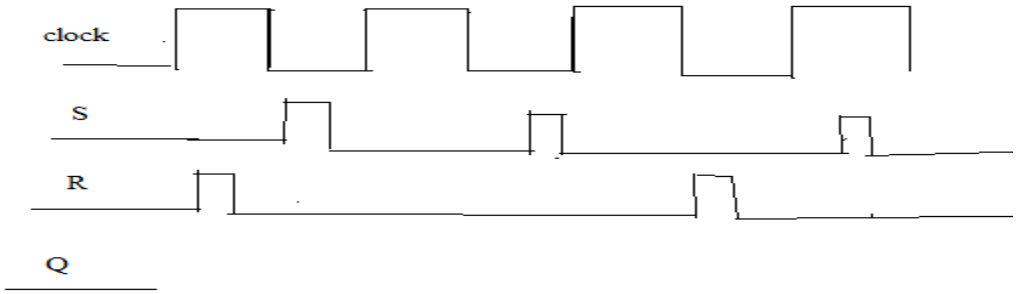
QUESTION FOUR

a) i) Draw the logic diagram of a T flip flop

ii) State any TWO applications of Flip flops (4marks)

b) With the aid of a logic diagram, Explain the operation of NOR gate leading edge triggered R-S flip-flop (10 marks)

c) Draw the outputs of fig 5 assuming leading edge triggered RS flip flop



2marks

d) with the aid of a diagram ,show how the TTL device is interfaced to a CMOS device(4 marks)

QUESTION FIVE

a) Define the following terms;

i) multiplexer ii) encoder (2 marks)

b) i) Draw the block diagram of a 4 to 1 line multiplexer and explain its operation
ii) State any TWO functions of the enable input of decoder
iii) State any TWO applications of a decoder (8 marks)

c) (i) Explain the term 'priority encoder'.
(ii) With the aid of a logic diagram, explain how decimal to BCD encoding is achieved with OR gates only. (10 Marks