THE MOMBASA POLYTECHNIC UNIVERSITY COLLEGE

Faculty of Engineering & Technology

DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY

HIGHER DIPLOMA IN COMPUTER STUDIES

STAGE ONE EXAMINATION

APRIL/MAY 2010 SERIES

COMPUTER ARCHITECTURE

TIME: 2 HOURS

Instructions to Candidates

1. This paper consists of **FIVE** Questions.
2. Section **A** Questions **ONE is COMPULSORY**.
3. Section **B** Answer **ONE** Question.
4. Section **C** Answer **ONE** Question.

SECTION A – Question ONE is Compulsory

Q1a) With the aid of a suitable diagram, describe the function of the Central Processing Unit. **[5 marks]**

b) Draw a clearly labeled A.L.U. block diagram and give a detailed description of its operation. **[5 marks]**

c) Explain clearly **five** single operand A.L.U operations and give **two** operand A.L.U operations. **[10 marks]**

d) Outline the Properties of Semiconductor memory **[4 marks]**

e) Explain the benefits of using multiple bus architecture as compared to a single bus. **[6 marks]**

SECTION B – Answer ONE only.

Q2a) The Central Process Unit cannot function without the input of control signals. Describe clearly at least **five** control signals. **[10 marks]**

b) With clearly labeled diagram, describe exhaustively the following Registers:

i. Accumulator
ii. The status Register. **[4 marks]**

c) i) Clearly Illustrate the Interconnection structures of the **three** major modules. **[7 marks]**

ii) Explain the **three** types of buses connecting the modules. **[6 marks]**

Q3a) i) Outline the function of any **five** Instruction types. **[5 marks]**

ii) Write an assembly language program to do the following:

- Load B register with immediate data 87H.
- Transfer this value into registers A and C.
- Load the D register with immediate data 2F H.
- Transfer this value to register E.
- Load the HL register pair with immediate data 8EF2 H.

[8 marks]

b) Translate the program into Machine Language starting at address 2000H.

[4 marks]

c) Find the final contents of the A register after the following assembly language has been run.

```
        MVI   A,      FC
LAB I : DCR  A
        JNZ  LAB I
        HALT
```

[3 marks]

SECTION C - Answer ONE only.

Q4) A combination circuit is used to control a seven-segment display of decimal digits. The circuit has four inputs, which provide the four-bit code used in packed decimal representation (0_{10} = 0000,...., 9_{10} = 1001). The seven out-puts define which segments will be activated to display a given decimal digit. Note that some combinations of inputs and outputs are not needed.

a. Develop a truth table for this circuit. **[8 marks]**
b. Provide an expression for any two of the seven segment outputs. **[6 marks]**

c. Draw the logic circuit implementation for the two expressions in (b) above. **[6 marks]**

Q5a) Design an algorithm for multiplying two n-bit numbers using suitable registers. **[6 marks]**

b) Write the logic diagram for the algorithm in a) above. **[6 marks]**

c) Provide an explanation on the principle of operation of the multiplier circuit. **[8 marks]**