## DIGITAL SYSTEMS DESIGN II [A]

## QUESTION ONE

a) (i) Define the micro operation as used with digital systems
(ii) Explain the FOUR categories of micro operations encountered in a digital system
(iii) Describe the following micro operation:

I $R_{0} \longleftarrow R_{1}+R_{2}$
II $R_{0} \longleftarrow R_{1}+R_{2}+1$
[10 marks]
b) Using full adder and associated combinational logic circuits of Figure Q1(b), design a 3 bit arithmetic circuit to perform the following:
When $S=0$ the circuit performs $F_{i}=A_{i}+B_{i}$
When $S=1$ the circuit performs $\boldsymbol{F}_{i}=\boldsymbol{A}_{i}-\boldsymbol{B}_{i}$


FIG. Q1(b)
[10 marks]
c) Explain the following THREE phases of hardware design of a digital system:
(i) System design
(ii) Logic design
(iii) Circuit design.
d) Describe the event that takes place as symbolised by the following micro operation statements:
i) $\mathrm{W}: \mathrm{M}[\mathrm{A} 1] \leftarrow \mathrm{B} 2$
ii) $\mathrm{R}: \mathrm{MBR} \leftarrow \mathrm{M}$
[4 marks]

## QUESTION TWO

a) With the aid of a diagram, explain the various parts of a digital computer system.
b) Differentiate between immediate addressing and direct addressing as used in a digital computer system
c) i) An 8-bit single computer requires 3 kilobytes of RAM and 2 kilobytes of ROM to operate. Assuming that ROM starts at memory location 0000 H followed immediately by RAM, draw the memory map for the system
(ii) Implement the memory in (i) using ROM chips of 512 X 4 and 512 X 8
[12 marks]

## QUESTION THREE

a) Design an arithmetic circuit with two selection variables $S_{1}$ and $S_{0}$ that generates the following arithmetic operations. Draw the logic diagram of two typical stages

| $S_{1}$ | $S_{0}$ | Operation | Function |
| :--- | :--- | :--- | :--- |
| 0 | 0 | $\mathrm{~F}=\mathrm{A}+\mathrm{B}$ | $\mathrm{F}=\mathrm{A}+\bar{B}+1$ |
| 0 | 1 | $\mathrm{~F}=\mathrm{B}-\mathrm{A}-1$ | $\mathrm{~F}=\mathrm{B}-\mathrm{A}$ |
| 1 | 0 | $\mathrm{~F}=\mathrm{A}-1$ | $\mathrm{~F}=\mathrm{A}+1$ |
| 1 | 1 | $\mathrm{~F}=\bar{A}$ | $\mathrm{~F}=\bar{A}+1$ |

[14 Marks]
b) With the aid of a diagram, explain the operation of a scratchpad memory used by a processor unit

## QUESTION FOUR

a) Assuming that the program counter contains the appropriate, opcode and using Instruction Register and Temporary Register, write the symbolic sequence of operation required to execute the following instruction:
(i) Add B to A
(ii) Add immediate operand to A [5 marks]
b) A processor unit employs a scratchpad memory. The processor consists of 64 registers of eight bits each. Determine
(i) The size of the scratchpad memory
(ii) The number of lines needed for the address
(iii) The number of lines the input data.
c) (i) The following relationships of the exclusive-OR operations are used in deriving the logic operations in an arithmetic logic unit. Prove that these relationships are valid:
I $\quad x \oplus 0=x$
II $\quad \mathrm{x} \oplus 1=\bar{x}$
III $\quad \mathrm{x} \oplus \bar{y}=x \odot y$
(ii) Explain in words the operations specified by the following register transfer operations:

I $\quad \mathrm{R} 3 \leftarrow \mathrm{R} 3-1$
II If $\left(S_{1}=1\right)$ then $R 0 \leftarrow R 1$ else if $\left(S_{2}=1\right)$ then $R 0 \leftarrow R 2$
III $\quad$ R2 $\leftarrow$ R2 +1 , R1 $\leftarrow \mathrm{R}$
[10 marks]

## QUESTION FIVE

a) Describe any FOUR addressing modes applicable to typical computer. [8 marks]
b) A typical processor unit is designed to consist of a register file with seven registers R1 through R7, two multiplexer to select bus A input and B input, a destination select decoder, an ALU and a shifter register and a status register.
(i) Draw a block diagram of processor unit with appropriate interconnection and describe its operation.
(ii) Draw the corresponding control word diagram and describe the function of each field
(iii) Give the bit values in the control word for the following micro-operation I $(\mathrm{R} 1 \leftarrow \mathrm{R} 1-\mathrm{R} 2)$
II (R2 $\leftarrow \mathrm{R} 4)$
[12 Marks]

