TECHNICAL UNIVERSITY OF MOMBASA

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION 2015/2016

UNIVERSITY EXAMINATIONS FOR THE DEGREE OF BACHELOR OF ELECTRICAL
AND ELECTRONIC ENGINEERING (BSEE)

EEE 2518   : DIGITAL SYSTEMS DESIGN I

TIME: 2 HOURS   **SERIES:** DECEMBER, 2015

INSTRUCTIONS TO CANDIDATES

1.   You are required to have the following for this examination;
   - Answer Booklet
   - A non Programmable Calculator

2.   This paper consists of **FIVE** Questions.

3.   Answer **ANY THREE** Questions.

4.   All Questions carry equal marks.

5.   **This paper consists of THREE papers printed.**

QUESTION ONE

a) Design a synchronous counter that counts as 000, 010, 101, 110, 000, 010, _ _ _ using J-K flip-flops. Ensure that the unused states of 001, 011, 100 and 111 go to 000 on the next clock pulse. What will the counter hardware look like if the unused states are to be considered as 'don't care's? Also determine the minimum number of same type gate ICs that can be used to implement both circuits.   (16 marks)

b) Determine the modulus of the counter and also the frequency of flip-flop Q_3 output.
                                                                        (**4 marks**)

QUESTION TWO

a) Show the logic arrangement of a PROM required to implement a 3 – bit odd parity generator. (**6 marks**)

b) Given two 2-bit binary numbers X_1X_0 and Y_1Y_0. Design a PLA device to implement a magnitude comparator to produce outputs for the two numbers. (**14 marks**)

QUESTION THREE

a) Using the top-down design procedure, obtain the realizable logic diagram for the above function. Assume, the available signals are ~F, A, ~B[NL], ~C[NL] and D[NL]. (**4 marks**)

b) Given the state diagram in Figure Q3, generate the state table and design a sequence circuit using T-flip flops. (**11marks**)
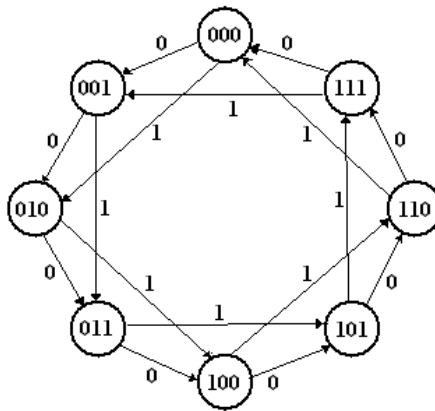

Figure Q3

c) Using a 4 – to – 1 multiplexer, implement the function

$$f(A, B, C, D) = \sum\nolimits_m (0,\ 2,\ 4,\ 7,\ 8,\ 10,\ 11, 12,\ 14, 15).$$ (**5 marks**)

QUESTION FOUR

a) State the design procedures for a Finite State Machine. (**5 marks**)
b) Determine the size of the PROM required for implementing the following logic circuits:
    i.   a binary multiplier that multiplies two four-bit numbers;
    ii.   a dual 8-to-1 multiplexer with common selection inputs;
    iii.   a single-digit BCD adder/subtractor with a control input for selection of operation.
(**7 marks**)

c) Develop a truth table of a Full adder and implement using 4 – to – 1 multiplexers with minimum external circuitry. (**8 marks**)

QUESTION FIVE

a) A circuit that controls a given digital system has three inputs: x_1, x_2 and x_3. It has to recognize three different conditions:

Condition A is true if x_3 is true and either x_1 is true or x_2 is false.
Condition B is true if x_1 is true and either x_2 or x_3 is false.
Condition C is true if x_2 is true and either x_1 is true or x_3 is false.
The control circuit must produce an output of 1 if at least two of the conditions A, B and C are true. Design the simplest circuit that can be used for this purpose. **(9 marks)**

b) Explain the functions of the following digital devices: Multiplexer, Decoder, Binary Comparator. **(6 marks)**

c) Obtain a Type-2 Multiplexer design to implement the following function. $F(A,B,C,D)=\Sigma_m(4,5,6,7,10,14)$. Signal List: ~F, ~A[NL], B[NL], C, D[NL]. **(5 marks)**