# TECHNICAL UNIVERSITY OF MOMBASA

**Faculty of Engineering and Technology**

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

**UNIVERSITY EXAMINATION 2016/2017**

UNIVERSITY EXAMINATIONS FOR THE DEGREE OF BACHELOR OF ELECTRICAL AND ELECTRONIC ENGINEERING (BSEE)

## EEE 2518 : DIGITAL SYSTEMS DESIGN I

**TIME:** 2 HOURS **SERIES:** DECEMBER, 2016

**INSTRUCTIONS TO CANDIDATES**

1. You are required to have the following for this examination;
   - Answer Booklet
   - A non Programmable Calculator
2. This paper consists of **FIVE** Questions.
3. Answer **ANY THREE** Questions.
4. All Questions carry equal marks.
5. **This paper consists of THREE printed pages.**

**QUESTION ONE**

a) Explain the general technique to design a divide by N ripple counter, assuming J-K flip-flops with preset available. (**5 marks**)

b) With aid of a transition table, design a modulo-5 D flip-flop based synchronous counter to repetitively count in the sequence 1, 3, 6, 2, 4, 1……. The unused states will assume a value represented by 2. Other than the flip-flop IC packages, use optimal IC packages. (**15 marks)**

**QUESTION TWO**

a) Develop a full SUBTRACTOR using NAND gates only and explain its operation.

(**10 marks**)

**b)** Using the tabular method minimization technique, obtain a minimum SOP expression for the function F (A, B, C, D, E) = $\sum_m$ = (2, 5, 6, 8, 9, 10, 11, 12, 17, 18, 19, 20, 21, 22, 24, 26, 27, 29, 30, 31) **(10 marks)**

## QUESTION THREE

a) Explain the functions of the following digital devices:

(i) Logic analyser

(ii) Binary comparator

(iii) Multiplexer (**6 marks**)

b) A certain building has a central heating system controlled by five thermostats in various locations. Each thermostat has a logic **1** output for too low a temperature, and logic **0** for too high temperature (thermostat cut off). Design NOR-to-NOR gate combinational networks to implement this specification. (**6 marks**)

c) Obtain realizable logic diagram for a 4-to-2 priority encoder for the following available signals ~$F_1$[NL], $F_0$, ~$I_2$[NL], $I_3$, $I_1$, $I_0$. Also implement it using minimum number of one type of gates. (**8 marks**)

## QUESTION FOUR

a) (i) State the design procedures for a sequential logic circuit.

(ii) Using a 4 – to – 1 multiplexer, implement the function

$f(A,B,C,D) = \sum_m (0,\ 2,\ 4,\ 5,\ 6,\ 7,\ 8,\ 10,\ 11,\ 12,\ 14).$ **(8 marks)**

b) Given the state diagram of Figure Q4b, generate the state table and design a sequential circuit using T-flip flops. (**12 marks**)

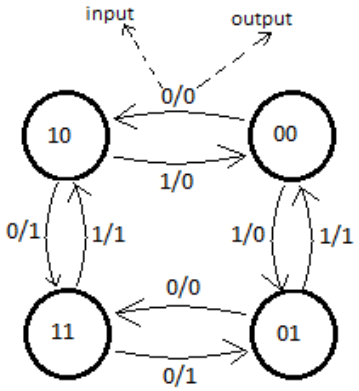

Figure Q4b

**QUESTION FIVE**

a) Design a PLA device that implements a 3-bit odd parity generation. (**8 marks**)

b) Design a logic circuit that has an enable input ‘E’ such that it converts a 3-bit binary value to its equivalent 3-bit gray code when E = 0 and when E = 1, it converts a 3-bit gray code to its binary equivalent. Implement using appropriate decoder and encoder with minimum external IC package. **(12 marks)**