

## TECHNICAL UNIVERSITY OF MOMBASA

## INSTITUTE OF COMPUTING AND INFORMATICS

# DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY

## **UNIVERSITY EXAMINATION FOR:**

## BACHELOR OF TECHNOLOGY IN INFORMATION COMMUNICATION TECHNOLOGY

EIT 4410: PARALLEL COMPUTING
EXAMINATION

**SERIES:** APRIL2017

TIME:2HOURS

DATE:5Sep2017

#### **Instructions to Candidates**

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **FIVE** questions. Attemptquestion ONE (Compulsory) and any other TWO questions.

Do not write on the question paper.

#### **QUESATION ONE (30 MARKS)**

- A. Distinguished between the following microprocessor performance metric measurements
- i. MIPS (Million Instructions per Second)

[5 marks]

ii. MHz (Millions of clock cycles per second)

[5 marks]

B. Von Neumann machine may refer to Von Neumann architecture, a conceptual model of computer architecture. IAS machine, a computer designed in the 1940s based on von Neumann's design. It is self-replicating machine, a class of machines that can replicate themselves. With an aid of a diagram discuss the following components of Von Neumann model

| i.   | Memory          | [5 marks] |
|------|-----------------|-----------|
| ii.  | Processing Unit | [5 marks] |
| iii. | Control Unit    | [5 marks] |
| iv.  | Input/output    | [5 marks] |

#### **QUESATION TWO (20 MARKS)**

As a hardware designer consultant for Xeon, you are required to design a set associative cache scheme of set size 4 blocks with the following memory cache parameters:

- a. Memory Size = 256KB
- b. Cache Size = 256KB
- c. Block Size 4B

Calculate the number of the following sections of address bit partitioning

| i.   | Offset bit   | [3 marks] |
|------|--|-----------|
| ii.  | Index bit  | [7 marks] |
| iii. | Tag bit  | [3 marks] |
| iv.  | Draw the design diagram for the Address Bit Partitioning | [7 marks] |

#### **QUESATION THREE (20 MARKS)**

Parallel programming model is an abstraction of parallel computer architecture, with which it is convenient to express algorithms and their composition in programs. The value of a programming model can be judged on its generality: how well a range of different problems can be expressed for a variety of different architectures, and its performance: how efficiently the compiled programs can execute. Discuss the following parallel programming models using relevant examples

| i.  | Shared Memory Model | [10 marks] |
|-----|---------------------|------------|
| ii. | Threads Model       | [10 marks] |

#### **QUESATION FOUR (20 MARKS)**

A. Describe briefly the MPI programing standard in parallel computing [5 marks]

B. Describe briefly the OpenMP programming standard in parallel computing [5 marks]

C. Write an enhanced "Hello World" MPI program using several MPI Environment Management routines in C Programming [10 marks]

#### **QUESATION FIVE (20 MARKS)**

Shared memory parallel computers vary widely, but generally have in common the ability for all processors to access all memory as global address space. Multiple processors can operate independently but share the same memory resources. Discuss the memory architecture and classes with respect to the following

i. Uniform Memory Access (UMA) [10 marks]ii. Non-Uniform Memory Access (NUMA) [10 marks]