TECHNICAL UNIVERSITY OF MOMBASA

FACULTY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF MEDICAL ENGINEERING

UNIVERSITY EXAMINATION FOR:

DIPLOMA IN MEDICAL ENGINEERING

EHL 2204: DIGITAL ELECTRONIC

END OF SEMESTER EXAMINATION

SERIES:APRIL2016

TIME:2HOURS

DATE:16May2016

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **FIVE** questions. Attemptquestion ONE (Compulsory) and any other TWO questions.

Do not write on the question paper.

Question ONE

1.(a)(i) State the DeMorgan's theorem

ii) Prove the DeMorgan's theorems using truth tables

(5 marks)

(b) i) Explain the advantage of Excess-3 code over the 8421 BCD code

ii) Name any THREE common types of error detection and correction codes

(5 marks)

(c) i) Show that $f = \overline{(a + \bar{b})(\bar{a} + b)}$ can be implemented using one Exclusive OR gate.

ii) Obtain the BCD equivalent of decimal 27 in 16-bit representation

(10 marks)

(d) i) State the TWO important characteristics that a designer must consider when selecting a logic family.

ii) List the SIX TTL subfamilies currently available.

iii) Give any TWO manufacturers suggestions that prevent damage from static discharge and transient's voltages, when working with CMOS ICs.

(10 marks)

Question TWO

(a) i) Name the two logic gates used to construct a half adder circuit.

ii) Draw the logic diagram of a full adder using the gates in 2a(i) above AND any other gate

(8 Marks)

(b) List for figure 1

i) the HA sum outputs for each set of input pulses shown.

ii) the half adder carry-out outputs for each set of input pulses shown.

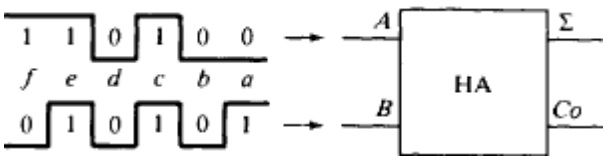

Figure 1

(12 marks)

Question THREE

(a) i) List the four synchronous modes of operation of the JK flip-flop

ii) Differentiate between Decade counters and Binary Coded Decimal (BCD) counters.

(8 Marks)

(b) Draw a logic diagram of a mod-8 ripple counter using JK flip-flops

(4 Marks)

(c) Refer to the binary ripple counter of Figure 2.

i) Obtain the modulus of the counter

ii) Determine the frequency of the ip-op Q3 output.

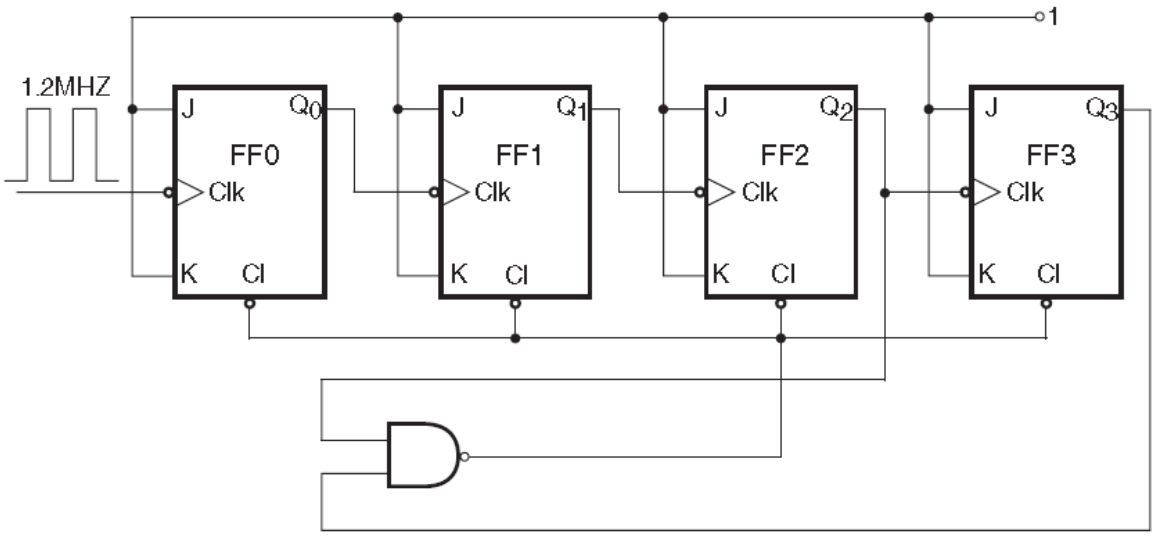

Figure 2

(8 marks)

Question FOUR

(a) i) Define radix of a number system

ii) Explain the reason for using hexadecimal number system representation for addresses and contents of memory locations.

(6 marks)

(b) The 7's complement of a certain octal number is 5264. Determine

i) it's binary equivalent

ii) its hexadecimal equivalent

(6 marks)

(c) Perform the following conversions

i) Eight-bit 2's complement representation of $(-23)_{10}$

ii) The decimal equivalent of $(00010111)_2$ represented in 2's complement form.

(4 marks)

(d) If a transmitting computer sends the 8-bit binary message 11000111 using an even parity bit. Write the 9-bit data with the parity bit in the most significant bit. If the receiving computer receives the 9-bit data as 110000111:-

i) State whether the 8-bit message received is correct

ii) Comment on your answer.

(4 marks)

Question FIVE

(a) Define the following as applied to Analogue to Digital converters (ADC)

i) Resolution

ii) Dynamic Range

(2 marks)

(b) An eight-bit D/A converter has a step size of 20 mV. Determine:-

i) the full-scale output

ii) percentage resolution.

(8 marks)

(c) i) With the aid of a binary ladder network describe the process of digital-to-analogue conversion.

ii) State TWO advantages of the method described in 5(c)(i) over the simple resistive network used for the same purpose

iii) Write an expression for the output analogue voltage for an n-bit binary ladder network.