TECHNICAL UNIVERSITY OF MOMBASA

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION FOR:

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEE2)

DIGITAL ELECTRONICS I

EEE 2102

END OF SEMESTER EXAMINATION

SERIES: MAY 2016

TIME: 2 HOURS

DATE: Pick DateSelect MonthPick Year

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **five** Questions;. Attempt any THREE Questions.

Do not write on the question paper.

QUESTION ONE

(i) Define the following terms.

a. Radix

b. Code (2 marks)

(ii) Carry out the following conversions.

i. 1110111.11_2 to decimal.

ii. $ACD2_{16}$ to decimal.

iii. 52.625_{10} to binary.

iv. 60.025_{10} to Octal. (10 marks)

(iii) Perform the following binary arithmetic operations:

i. 11101 + 1110. (2 marks)

ii. 88 + 52 in BCD (2 marks)

iii. 11011 X 11010 (2 marks)

iv. 1110100 ÷101. (2 marks)

QUESTION TWO

a. Work out:

(i) $23_{10} - 76_{10}$ using 2's compliment.

(ii) $55_{10} - 45_{10}$ using 1's compliment. (8 marks)

b. Distinguish between weighted and unweighted code and give an example of each. (4 marks)

c. Use the ASCII table attached to decode the following sequence.

0110111 1000011 1000001 1010100 1010011 0111111 (3 marks)

d. Encode the following characters using ASCII table:

(i) @

(ii) %

(iii) # (3 marks)

e. Convert the gray code 1111001100 to binary. (2 marks)

QUESTION THREE

a. The arithmetic combination of lock circuitry for four gates at **Technical University of Mombasa (TUM)** is to be installed. A warning in the control room will sound if the following conditions occurs:
   - ✓ Gate **A, D** are open.
   - ✓ Gate **C** is closed and **A, B, D** are open.
   - ✓ Gate **A, C** are open.
   - ✓ Gate **C, D** are closed while **A, B** are open.
   - ✓ Gate **C, D** are open while **A, B** are closed.
   - ✓ Gate **A, B** are closed but **C, D** are open.
   - ✓ Gate **B** is closed while **A, C, D** are open.

   Take **closed** = HIGH (**1**) and
   Open = LOW (**0**)

   (i) Write down the truth table of the circuit.
   (ii) Use K map to get a reduced function.
   (iii) Implement the reduced function using **NAND** gates only. (11 marks)

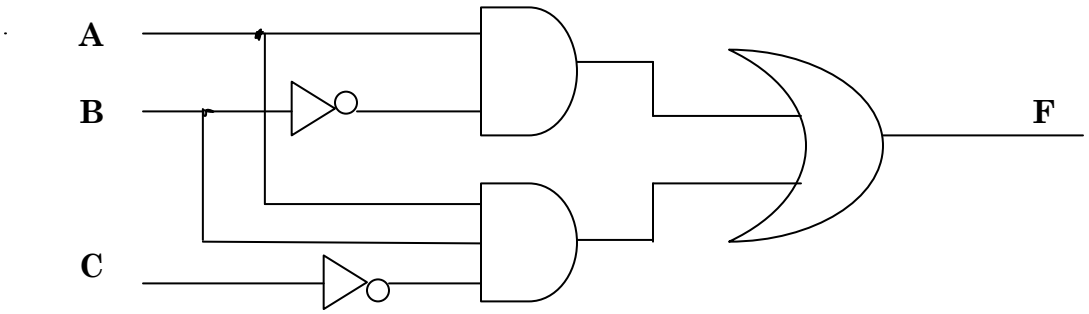
b. State four applications of Logic gates. (4 marks)

c. Two electrical signals represented by $A = 101101$ and $B = 110101$are applied to a 2-input AND gate. Sketch the output signal and the binary number it represents. (3 marks)

d. State Demorgans theorem. (2 marks)

QUESTION FOUR

(i) Determine the function F from the figure Q4.i (2marks)



(ii) Give the following logic expression as a function of minterms and hence simplify using a K-map.

$Z = A\bar{B} + \bar{A}CD + \bar{A}\bar{B}C + A\bar{B}C\bar{D}$ (5 marks)

(iii) Draw the table of excess -3 code against the decimal 0-9. (3 marks)

(iv) Prove the following Boolean identities:

i. $AC + ABC = AC$

ii. $A + \bar{A}B = A + B$

iii. $ABC + A\bar{B}C + AB\bar{C} = A(B + C)$ (7 marks)

(v) Simplify the following expressions using Boolean Algebra: (3 marks)

a) $Y = \overline{(\overline{A + B}) + (\overline{C + D})}$

b) $Y = \overline{(A + \bar{B})} + \overline{(AB)}$

QUESTION FIVE

(i) The truth table of a logic circuit is as shown in the table Q5. Synthesize the circuit with a minimum number of NAND gates. (7 marks)

Inputs			Outputs	
A	B	C	Y_1	Y_2
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

(ii) Name examples of saturated logic families. (2 marks)

(iii) Differentiate between Positive logic and negative logic. (4 marks)

(iv) What function of asynchronous inputs of a flip flop? (1 mark)

(v) Give **two** examples of non-saturated logic families. (2 marks)

(vi) Define the time flip flop and hence explain the operation of a latch with the use of a truth table. (4 marks)