TECHNICAL UNIVERSITY OF MOMBASA

# Faculty of Engineering and Technology <br> DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING <br> UNIVERSITY EXAMINATION FOR: <br> CERTIFICATE IN ELECTRICAL POWER ENGINEERING (CEPE 2) <br> DIGITAL ELECTRONICS I 

EEE 1102
END OF SEMESTER EXAMINATION
SERIES: MAY 2016

TIME: 2 HOURS

## DATE:Pick DateSelect MonthPick Year

## Instructions to Candidates

You should have the following for this examination
-Answer Booklet, examination pass and student ID
This paper consists of five Questions;. Attempt any THREE Questions.
Do not write on the question paper.

## QUESTION ONE

a. Define the following terms.
(i) Radix
(ii) Code
b. Carry out the following conversions.
(i) $1110111.01_{2}$ to decimal.
(ii) $\mathrm{AC} 2_{16}$ to decimal.
(iii) $52.625_{10}$ to binary.
(iv) $48.125_{10}$ to Octal.
c. Perform the following binary arithmetic operations:
i. $11101+1110$ ( 2 marks)
ii. $11110-11011$.
( 2 marks)
iii. $\quad 11011 \times 1100$
(2 marks)
iv. $1110100 \div 101$.
(2 marks)

## QUESTION TWO

a. Work out:
a. $23_{10}-76_{10}$ using 2 's compliment.
b. $45_{10}-55_{10}$ using 1 's compliment.
(8 marks)
b. Distinguish between weighted and unweighted code and give an example of each.
c. Use the ASCII table attached to decode the following sequence.
$\begin{array}{llllll}0110111 & 1000011 & 1000001 & 1010100 & 1010011 & 0111111\end{array}$
(3 marks)
d.Encode the following characters using ASCII table:
(i) @
(ii) \%
(iii) \#
e. Convert the gray code 1111001100 to binary.

## QUESTION THREE

a. Perform the following code arithmetic:
i. $88+52$ in BCD .
ii. $8-2$ in excess 3 BCD .
b. Three sensors are used to monitor pressure $\mathbf{P}$, temperature $\mathbf{T}$, and voltage $\mathbf{V}$ of an industrial plant. An alarm $\mathbf{X}$ should sound for the following conditions:
$>$ If both temperature and voltage sensors are OFF.
> If temperature sensor is $\mathbf{O N}$ and voltage sensor is OFF.
> If pressure sensor is OFF and voltage sensor is ON.

Take $\mathbf{O N}=$ Logic $\mathbf{1}$
$\mathbf{O F F}=$ Logic $\mathbf{0}$

Required:
i. Develop a truth table for the problem.
ii. Obtain the Boolean expression relating PTV and X.
iii. Minimize the expression using Karnaugh Map.
iv. Implement the minimized expression using basic gates. (10 marks)
c. An office building has an elevator system consisting of three elevators $\mathrm{A}, \mathrm{B}$ and C. A logic circuit is required that will provide an alarm any time two of the three elevators is in use.
i. Draw the truth table to satisfy the given conditions.
ii. Derive the expressions for the sum of products.
iii. Hence draw the simplified logic circuit.

## QUESTION FOUR

a. Draw the table of excess -3 code against the decimal 0-9.
(3 marks)
b. Design from first principles the full adder binary circuit using logic gates.
(6 marks)
c. Prove the following Boolean identities:
i. $A C+A B C=A C$
ii. $\quad \mathrm{A}+\overline{\mathrm{A}} \mathrm{B}=\mathrm{A}+\mathrm{B}$
iii. $\quad A B C+A \bar{B} C+A B \bar{C}=A(B+C)$
d. Simplify the following expressions using Boolean Algebra:
(4 marks)
(i) $\mathrm{Y} \overline{\overline{=(\mathrm{A}}+\mathrm{B}) \overline{+(\mathrm{C}}}+\mathrm{D})$
(ii) $\overline{\mathrm{Y}}=\overline{(\overline{\mathrm{A}}+\mathrm{B})+(\mathrm{AB})}$

## QUESTION FIVE

(i) State Demorgans theorem.
(ii) Prove by truth table that:

$$
\begin{equation*}
A+1=1 \tag{2marks}
\end{equation*}
$$

(iii) Two electrical signals represented by $A=101101$ and $B=110101$ are applied to a 2 -input AND gate. Sketch the output signal and the binary number it represents.
(3 marks)
(iv) Give the following logic expression as a function of minterms and hence simplify using a K-map.

$$
\begin{equation*}
\mathrm{Z}=\mathrm{A} \overline{\mathrm{~B}}+\overline{\mathrm{A}} \mathrm{CD}+\overline{\mathrm{A}} \overline{\mathrm{~B}} \mathrm{C}+\mathrm{A} \overline{\mathrm{~B}} \mathrm{C} \overline{\mathrm{D}} \tag{6marks}
\end{equation*}
$$

(v) The truth table of a logic circuit is as shown in the table Q5. Synthesize the circuit with a minimum number of NAND gates. (7 marks)

|  | Inputs |  | Outputs |  |  |
| :--- | :---: | :---: | :--- | :---: | :---: |
| A | B | C | $\mathrm{Y}_{1}$ |  | $\mathrm{Y}_{2}$ |
| 0 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 0 | 1 |  |
| 0 | 1 | 0 | 1 | 1 |  |
| 0 | 1 | 1 | 1 | 0 |  |
| 1 | 0 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 1 | 1 |  |
| 1 | 1 | 0 | 1 | 0 |  |
| 1 | 1 | 1 | 0 | 0 |  |

