



TECHNICAL UNIVERSITY OF MOMBASA

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION FOR:

CERTIFICATE IN ELECTRICAL POWER ENGINEERING (CEPE 3)

DIGITAL ELECTRONICS II

EEE 1203

END OF SEMESTER EXAMINATION

SERIES: MAY 2016

TIME: 2 HOURS

DATE: Pick Date Select Month Pick Year

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **five** Questions;. Attempt any **THREE** Questions.

Do not write on the question paper.

QUESTION ONE

a. Define the following terms.

- a. Current sinking.
- b. Current sourcing.
- c. Positive logic.
- d. Negative logic.
- e. Noise margin.

(10 marks)

b. A unit load for some particular logic family is as follows.

$$1 \text{ UL} = 50\mu\text{A} \quad \text{HIGH state.}$$

$$1 \text{ UL} = 10\text{mA} \quad \text{LOW state.}$$

Determine the fan-in and fan-out for a gate in this family that has the following parameters.

$$I_{OH} = 300\mu\text{A}$$

$$I_{OL} = 20\text{mA}$$

$$I_{IH} = 120\mu\text{A}$$

$$I_{IL} = 1\text{mA}$$

(4 marks)

c. State and explain any three Logic families.

(3 marks)

A TTL logic gate draws 1mA when its output is **HIGH** and 2.15 mA when its output is **LOW**. Calculate the average power dissipation if the supply voltage is 8V and the Logic gate is operated on 50% duty cycle.

(3 marks)

QUESTION TWO

a. With the aid of a diagram describe the operation of RTL.

(6 marks)

b. State four characteristics of DTL.

(4 marks)

c. An office building has an elevator system consisting of three elevators X, Y and Z. A logic circuit is required that will provide an alarm any time two of the three elevators is in use.

i. Draw the truth table to satisfy the given conditions.

ii. Derive the expressions for the sum of products.

(4 marks)

d. Decode the following 7-bit ASCII message.

11100100 1001001 1110100

(3 marks)

e. State **TWO** advantages and **ONE** disadvantage of CMOS over TTL.

(3 marks)

QUESTION THREE

a. Explain one method of interfacing TTL to drive CMOS devices.

(2 marks)

- b. Distinguish between the following as applied to sequential circuits.
- i. Asynchronous and synchronous.
 - ii. Setup and hold time. (4 marks)
- c. State the functions of the asynchronous inputs of a clocked flip flop. (2 marks)
- d. State one advantage of the JK flip flop over the RS flip flop. (2 marks)
- e. Three sensors are used to monitor humidity H, viscosity V, and flow rate R of an industrial plant. An alarm Y should sound for the following conditions:
- If both viscosity and flow rate sensors are OFF.
 - If viscosity sensor is ON and flow rate sensor is OFF.
 - If humidity sensor is OFF and flow rate sensor is ON.

Take ON = Logic 1

OFF = Logic 0

Required:

- i. Develop a truth table for the problem.
- ii. Obtain the Boolean expression relating XVR and Y.
- iii. Minimize the expression using Karnaugh Map.
- iv. Implement the minimized expression using basic gates. (10 marks)

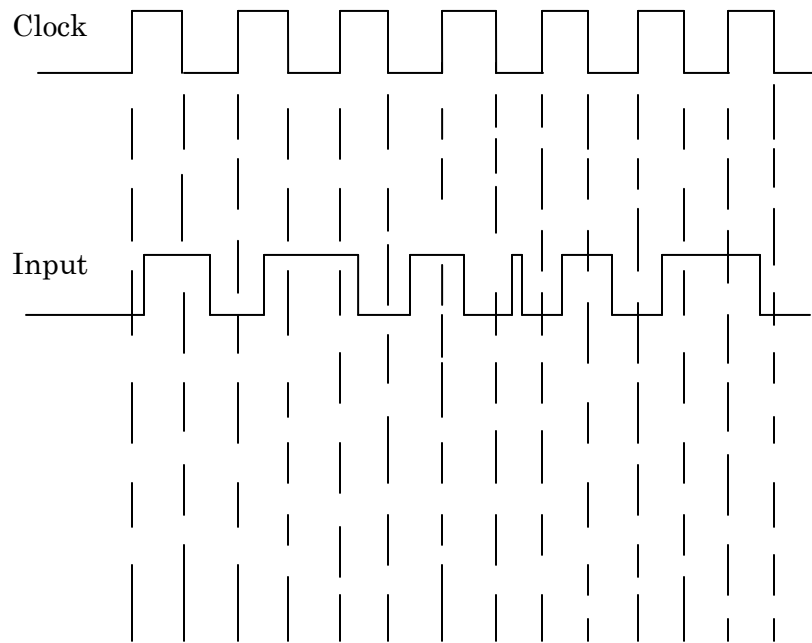
QUESTION FOUR

- a. Draw the logic diagram of 4-bit even parity checker using NAND gates and explain its operation with the help of Truth table. (7 marks)
- b. Design and implement a 3 bit odd parity checker generator. (6 marks)
- c. With the aid of a diagram explain the operation of a latch. (4 marks)

- d. State **THREE** applications of flip flops. (3 marks)

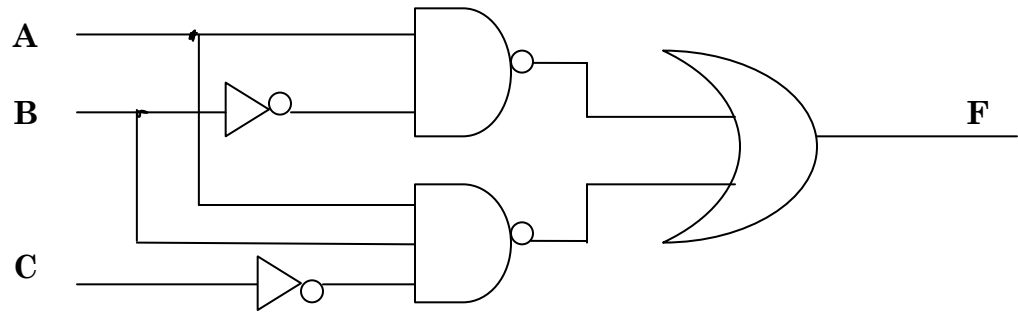
QUESTION FIVE

- a. The clock and the input waveforms shown below are applied to the D input of a positive edge triggered D flip flop. Sketch the output waveforms. (4 marks)



- b. Design a MOD-5 synchronous counter using J-K Flip-Flops. (8 marks)

- c. Determine the function F from the figure Q4.i (3marks)



- d. State any **THREE** applications of CMOS devices. (3 marks)
- e. State any **TWO** precautions to be considered when handling mosfets. (2 marks)