TECHNICAL UNIVERSITY OF MOMBASA

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATION FOR:

CERTIFICATE IN ELECTRICAL POWER ENGINEERING (CEPE 3)

DIGITAL ELECTRONICS II

EEE 1203

END OF SEMESTER EXAMINATION

SERIES: MAY 2016

TIME: 2 HOURS

DATE: Pick DateSelect MonthPick Year

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **five** Questions;. Attempt any THREE Questions.

Do not write on the question paper.

QUESTION ONE

a. Define the following terms.

   a. Fan in.
   b. Fan out.
   c. Propagation delay.
   d. Noise immunity.
   e. Noise margin. (10 marks)

b. A unit load for some particular logic family is as follows.

   1 UL = 60μA HIGH state.
   1 UL = 1mA LOW state.

   Determine the fan-in and fan-out for a gate in this family that has the following parameters.

   I_{OH} = 400μA
   I_{OL} = 10mA
   I_{IH} = 150μA
   I_{IL} = 4mA (4 marks)

c. State and explain any three Logic families. (3 marks)

d. A TTL logic gate draws 2mA when its output is **HIGH** and 3.5 mA when its output is **LOW.** Calculate the average power dissipation if the supply voltage is 5V and the Logic gate is operated on 50% duty cycle. (3 marks)

QUESTION TWO

(i) With the aid of a diagram describe the operation of DTL. (6 marks)

(ii) Differentiate between:
   i. Positive logic and negative logic.
   ii. Current sinking and current sourcing. (4 marks)

(iii) State four characteristics of RTL. (4 marks)

(iv) An office building has an elevator system consisting of three elevators A, B and C. A logic circuit is required that will provide an alarm any time two of the three elevators is in use.
   i. Draw the truth table to satisfy the given conditions.
   ii. Derive the expressions for the sum of products. (4 marks)

(v) Decode the following 7-bit ASCII message.
10100100 1000001 1010100 (2 marks)

QUESTION THREE

a. State three advantages and one disadvantage of CMOS over TTL. (4 marks)
b. Explain one method of interfacing TTL to drive CMOS devices. (2 marks)
c. Distinguish between the following as applied to sequential circuits.
   i. Asynchronous and synchronous.
   ii. Sequential and combinational logic circuits. (4 marks)
d. Three sensors are used to monitor pressure **P**, temperature **T**, and voltage **V** of an industrial plant. An alarm **X** should sound for the following conditions:

- If both temperature and voltage sensors are **OFF**.
- If temperature sensor is **ON** and voltage sensor is **OFF**.
- If pressure sensor is **OFF** and voltage sensor is **ON**.

Take **ON** = Logic **1**

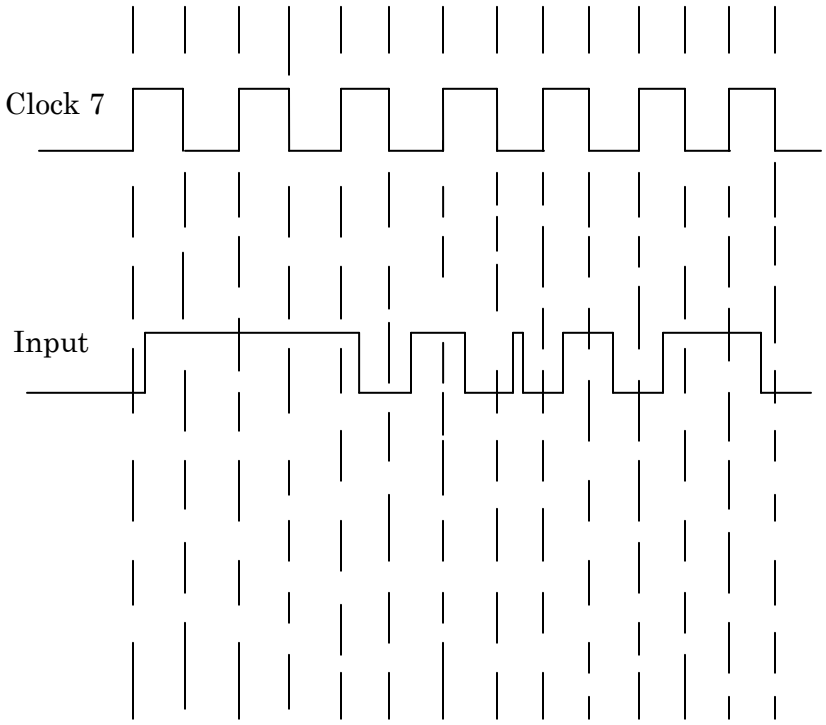
OFF = Logic **0**

Required:

i. Develop a truth table for the problem.
ii. Obtain the Boolean expression relating **PTV** and **X**.
iii. Minimize the expression using Karnaugh Map.
iv. Implement the minimized expression using basic gates. (10 marks)

QUESTION FOUR

a. The clock and the input waveforms shown below are applied to the D input of a positive edge triggered D flip flop. Sketch the output waveforms. (4 marks)



b. Design a MOD-6 synchronous counter using J-K Flip-Flops. (8 marks)

c. Determine the function F from the figure Q4.i (3marks)

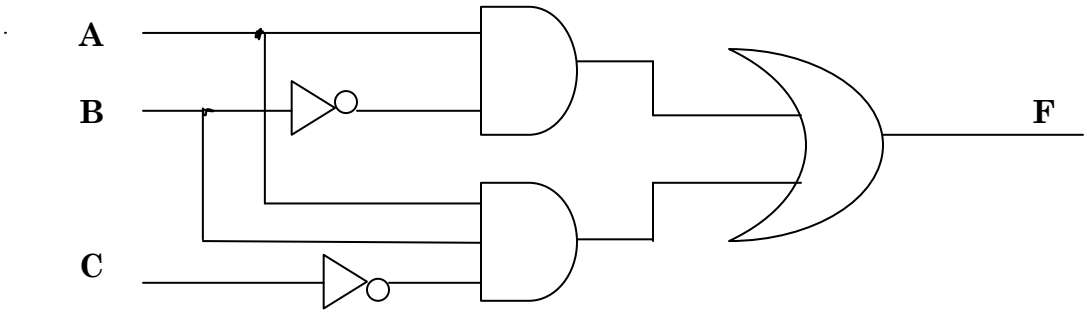


Fig.Q4.c

d. State any **THREE** applications of CMOS devices. (3 marks)

e. State any **TWO** precautions to be considered when handling mosfets. (2 marks)

QUESTION FIVE

a. Draw the logic diagram of 4-bit odd parity checker using EX-NOR gates and explain its operation with the help of Truth table. (7 marks)

b. Design and implement a 3 bit even parity checker generator. (6 marks)

c. With the aid of a diagram explain the operation of a latch. (4 marks)

d. State **THREE** applications of flip flops. (3 marks)