# TECHNICAL UNIVERSITY OF MOMBASA

***Faculty of Engineering and Technology***

**DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING**

## UNIVERSITY EXAMINATION FOR:

**CERTIFICATE IN ELECTRICAL POWER ENGINEERING (CEPE 2)**

**DIGITAL ELECTRONICS I**

**EEE 1102**

END OF SEMESTER EXAMINATION

**SERIES: MAY 2016**

**TIME:** 2 HOURS

**DATE:**Pick DateSelect MonthPick Year

**Instructions to Candidates**

You should have the following for this examination

*-Answer Booklet, examination pass and student ID*

This paper consists of **five** Questions;. Attempt any THREE Questions.

**Do not write on the question paper.**

## QUESTION ONE

a. Define the term code. (2 marks)

b. Carry out the following conversions.

(i) $010011.01_2$ to decimal.
(ii) $ACD4_{16}$ to decimal.
(iii) $25.125_{10}$ to binary.
(iv) $48.125_{10}$ to Octal. (10 marks)

c. Perform the following binary arithmetic operations:

i. 10101 + 1010. ( 2 marks)
ii. 111101 - 11010. ( 2 marks)
iii. 11011 x 1110 (2 marks)
iv. 1010101 ÷100. (2 marks)

## QUESTION TWO

a. Work out:

(i) $47_{10} - 25_{10}$ using 2's compliment.
(ii) $27_{10} - 37_{10}$ using 1's compliment. (8 marks)

b. Distinguish between weighted and unweighted code and give an example of each. (4 marks)

c. Use the ASCII table attached to decode the following sequence.

0110111 1000011 1000001 1010100 1010011 0111111
(3 marks)

d. Encode the following characters using ASCII table:

a. @

b. % (2 marks)

e. Convert the gray code 1111001100 to binary. (3 marks)

## QUESTION THREE

a. The arithmetic combination of lock circuitry for four gates at **Technical University of Mombasa (TUM)** is to be installed. A warning in the control room will sound if the following conditions occurs:
   - ✓ Gate **A, D** are open.
   - ✓ Gate **C** is closed and **A, B, D** are open.
   - ✓ Gate **A, C** are open.
   - ✓ Gate **C, D** are closed while **A, B** are open.
   - ✓ Gate **C, D** are open while **A, B** are closed.
   - ✓ Gate **B** is closed while **A, C, D** are open.

   Take **closed** = HIGH (**1**) and
   **Open** = LOW (**0**)

   (i) Write down the truth table of the circuit.
   (ii) Use K map to get a reduced function.
   (iii) Implement the reduced function using **NAND** gates only. (11 marks)

b. State **four** applications of Logic gates. (4 marks)

c. Two electrical signals represented by $A = 101101$ and $B = 110101$are applied to a 2-input AND gate. Sketch the output signal and the binary number it represents. (3marks)

d. State Demorgans theorem. (2 marks)

## QUESTION FOUR

(i) An office building has an elevator system consisting of three elevators **A, B** and **C. A** logic circuit is required that will provide an alarm any time **TWO** of the three elevators is in use.

   a. Draw the truth table to satisfy the given conditions.
   b. Derive the expressions for the sum of products. (4 marks)

(ii) Give the following logic expression as a function of minterms and hence simplify using a K-map.

$$Z = A\bar{B} + \bar{A}CD + \bar{A}\bar{B}C + A\bar{B}C\bar{D}$$ (4 marks)

(iii) Draw the table of gray code against the decimal 0-9. (3 marks)

(iv) Prove the following Boolean identities:

i. $XZ + XYZ = XZ$

ii. $X + \widetilde{X}Y = X + Y$

iii. $XYZ + X\overline{Y}Z + XY\overline{Z} = X(Y + Z)$ (5 marks)

(v) Simplify the following expressions using Boolean Algebra: (4 marks)

a) $A = \overline{(\overline{W + X}) + (\overline{Y + Z})}$

b) $B = \overline{(X + \overline{Y})} + \overline{(XY)}$

**QUESTION FIVE**

a. The correct functioning of a machine is monitored by three **LED** indicators named **A**, **B**, and **C**. the machine is working if one of the following conditions holds.
   - **ALL LED** are Red.
   - **A** is red and either **B** or **C** is green.
   - **C** is red and **A** is green.

   i. Draw the truth table and produce a Boolean expression to represent when the machine is working. (3 marks)

   ii. Implement the expression in (i) above using basic gates only. (4 marks)

b. Draw the table of **excess -3 code** against the **decimal 0-9.** (3 marks)

c. Design from first principles the full adder binary circuit using logic gates. (5 marks)

d. Design and implement a 3 bit even parity checker generator. (5 marks)