TECHNICAL UNIVERSITY OF MOMBASA

INSTITUTE OF COMPUTING AND INFORMATICS

DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY

UNIVERSITY EXAMINATION FOR:

(BTIT14S J-FT & BSIT 14S J-FT)

ICS 2205: EEE 4250: DIGITAL LOGIC & DIGITAL ELECTRONICS

END OF SEMESTER EXAMINATION

SERIES:APRIL2016

TIME:2HOURS

DATE: Pick DateMay2016

Instructions to Candidates

You should have the following for this examination

-Answer Booklet, examination pass and student ID

This paper consists of **FIVE** questions. Attempt question ONE (Compulsory) and any other TWO questions.

Do not write on the question paper.

Question ONE

a) State and prove De Morgan's theorem. (8 Marks)

b) Differentiate between the following terms
   i. Basic logic gates and Universal logic gates
   ii. Combinational circuits and sequential circuits
   iii. Level triggered and edge triggered (6 Marks)

c) Prove using the truth table $\bar{A}.B + A.\bar{B} + A.B = A + B$ (4 Marks)

d) Perform the following arithmetic using 2's complement
   i. 36 + 24
   ii. 43 - 34
   iii. 36 - 42 (6 Marks)

e) Design and implement a 3-bit majority function. (6 Marks)

Question TWO

a) Design the logic circuit of a 2 bit comparator to give the greater than, equality and less than functions at the output. (14 Marks)

b) Using NAND gates only implement the equality function. (6 Marks)

Question THREE

a) Design the logic circuit of a full adder circuit. (8 Marks)

b) Using the full adder implement a 4-bit adder circuit (6 Marks)

c) Provide the additional logic gates that may be included to convert the full adder circuit to a 4 bit adder/subtract circuit. (6 Marks)

Question FOUR

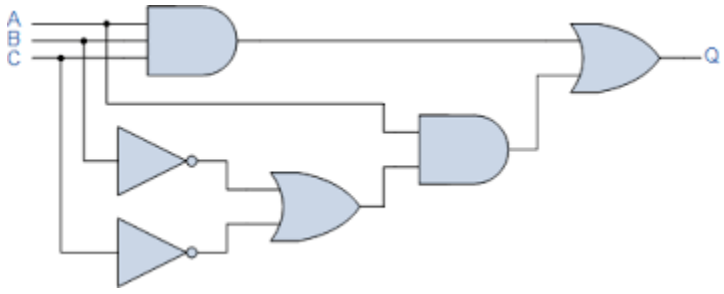
a) Use Boolean Identities to simplify

i) $X = \bar{A}.\bar{B}.\bar{C} + \bar{A}.\bar{B}.C + A.\bar{B}.\bar{C} + A.\bar{B}.C$

ii) $Y = (A + \bar{B} + \bar{C}).(A + \bar{B}.C)$

iii) $Y = (A + B.A) + \overline{(C + D + E.\overline{\overline{C}})}$ (9 Marks)

b) The logic circuit below implements the function Q.



i. Generate the Boolean expression for the function Q
ii. Simplify the expression for Q
iii. Implement using NAND gates only (11 Marks)

Question FIVE

a) Describe the operation of a J-K flip flop. (6 Marks)

b) Using a J-K flip flop construct a 4-bit counter. (6 Marks)

c) Show the additional logic that need to be added to build a module 10 counter. (4 Marks)

d) Describe propagation delay and the hazards associated with the delay. (4 Marks)