THE MOMBASA POLYTECHNIC UNIVERSITY COLLEGE

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DEPE 2
DTIE E
DEAE 2

EET 3123

DIGITAL ELECTRONICS I

SEMESTER II EXAMINATIONS

SERIES: FEBRUARY 2011 SERIES

TIME: 2 HOURS

Instructions to Candidates:

Question ONE

a) i) State any TWO differences between gray and straight binary codes.
ii) Convert 101100_2 to gray code
iii) Perform the following arithmetic using EX-3 BCD 1000-0010. (6 marks)

b) Three sensors are used to monitor pressure (P), Temperature (T) and voltage (V) of an industrial plant. An alarm should sound for the following conditions;

- If both temperature and voltage sensors are OFF
- If temperature sensor is ON and voltage sensor is OFF
- If pressure sensor is OFF and voltage sensor is ON.

Take a sensor ON = logic 1 and OFF = logic 0.

i) Develop a truth table for the problem
ii) Plot these conditions on a Karnaugh map
iii) Determine the minimized expression
iv) Draw the logic circuit that corresponds to the minimized expression. (6 marks)

c) i) Implement using NOR gates only the function $F = (A + B)\overline{C}$
ii) Determine the Boolean expression of fig 1 and reduce it using Boolean algebra.

Fig 1 (7 marks)

d) i) Draw the logic circuit and truth table of a J-K flip-flop
ii) State the advantages of J-K over the R-S flip-flop. (4 marks)

e) i) Explain the operation of the circuit of fig 2.

Fig 2

ii) State any TWO advantages and ONE disadvantage of CMOS compared to TTL logic devices. (7 marks)

Question TWO

a) i) Define the following terms:
   I) radix
   II) weight
   ii) Perform the following conversions
   I) 42.3125_{10} to binary
   II) 110101.1010_2 to decimal
   III) 473_8 to hexadecimal
   IV) 357_8 to decimal
   V) 110110101 gray to binary. (12marks)

b) Perform the following operations
   i) $BA_{16} + A5_{16}$
   ii) 1000 1000 + 0101 0010 in BCD
   iii) -8-7 using 1;s complement addition
   iv) 15-9 using 2's complement addition (8 marks)

Question THREE

a) i) State Demorgan's theorem
   ii) Simplify the following expressions using Boolean algebra
   I) $F = \overline{A\overline{B}C + AB\overline{C} + ABC}$
   II) $F = (\overline{A} + B)(A + \overline{B} + C)$
   iii) From table 1, determine:

A	B	C	F
0	1	0	1
1	0	0	0
1	0	1	1
1	1	0	0

(10marks)

b) Minimize the following expressions using Karnaugh maps
   i) $F = A\overline{C}D + \overline{A}B\overline{C}D + \overline{A}\overline{B}D + A\overline{B}CD$
   ii) $F = AB\overline{C} + \overline{A}BC + A\overline{B}\overline{C} + \overline{A}\overline{C}$ (8 marks)

c) Show that
$F = \overline{A..\overline{BC}} = \overline{A} + BC$ (2 marks)

Question FOUR

a) Define the following terms:
   i) fan out
   ii) noise immunity
   iii) propagation delay (3 marks)

b) i) State any TWO advantages and any ONE disadvantage of totem pole output in TTL devices.
   ii) Explain why it is not advisable to leave unused inputs of a TTL device floating.
   iii) State any TWO ways of overcoming the problem in (b) (ii) above.
   iv) Explain the operation of the circuit in fig 3.

Fig 3

c) A unit load (uL) for a logic family is as follows:

1uL = 40µA high state and
= 1.5mA low state

If high state output current I_{OH} = 360µA and low state output current I_{OL} = 12mA, determine the fan out. (3 marks)

Question FIVE

a) Distinguish between the following sequential logic circuits
   i) synchronous
   ii) asynchronous (2 marks)

b) i) Explain the term race condition and state how it is minimized.
   ii) Draw the logic diagram of a T flip flop
   iii) With the aid of a logic diagram, explain the operation of NOR gate leading edge triggered R-S flip-flop. (14marks)

c) i) The waveforms of a fig 4 apply to a trailing edge triggered J-K flip flop. Draw the waveforms for the outputs Q and $\overline{Q}$. Assume that Q is initially at logic 0.
   ii) State any TWO applications of flip flops. (4 marks)

Fig 4