THE MOMBASA POLYTECHNIC UNIVERSITY COLLEGE

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DIPLOMA IN TECHNOLOGY
Electronics Engineering
Electrical Power Engineering
Electronics & Automation Engineering
Telecommunication and Information Engineering
Computer Science Engineering
Instrumentation and Control Engineering

EEE 32106   :   DIGITAL ELECTRONICS I

SEMESTER I EXAMINATIONS

SERIES: SEPTEMBER/OCTOBER 2010

TIME: 2 HOURS

Instructions to Candidates:

1.   You are required to have the following for this examination;
   - Answer booklet
   - A non-programmable scientific calculator

2.   Answer Question **ONE (COMPULSORY)** and any other **TWO** Questions.

Question ONE

(a)   Perform the following arithmetic operations:

   (i) $1101110_2 + 10111_2$

   (ii) $11101_2 \times 1101_2$

            $A51_{16} + 236_8$ (leave the answer in Hexadecimal)

                                                                          (7 Marks)

(b)   (i)   State Demogans theorem's.

   (ii)   Prove using Boolean algebra that:

   $$\overline{\overline{A} + \overline{B} + ABC} + \overline{A\overline{B}C} = 1$$

   (iii)   Simplify and implement using NAND gates only the function:

   $$\overline{\overline{AB} + \overline{B\overline{C}D}}$$

   (iv)   A control circuit is used in an illumination plant to control three lights. It operates
            when atleast any **TWO** of the **THREE** lights are **ON.**

            (I)   Draw the truth table for the conditions.
            (II)   Derive the sum of products expression.

                                                                          (12 Marks)

(c)   (i)   Show any **ONE** method of interfacing CMOS to TTL gates.

   (ii)   State any **TWO** advantages and **ONE** disadvantage of CMOS over TTL.

                                                                          (5 Marks)

(d)   With the aid of a truth table explain the operation of the circuit in fig. 1.   **(6 Marks)**

(ANSWER ANY OTHER TWO QUESTIONS)

Question TWO

(a)   (i)   Explain the following terms:

        (I)   Maxterms

        (II)   Minterms

(4 Marks)

    (ii)   Simplify the following using Boolean algebra.

        (I) $F = X\overline{Y}Z + xy\overline{Z} + xYZ$

        (II) $\boldsymbol{P = \overline{(\overline{A} + \overline{B})(\overline{\overline{A}.\overline{B}.C})}}$

(6 Marks)

(b)   An Engine has **FOUR (4)** fail Sensors. The engine should keep running
    unless any of the following conditions arise:

- If sensor 2 is activated.

- If sensor 1 and 3 are activated at the same time.

- If sensor 2 and 3 are activated at the same time.

- If sensor 1, 3, 4 and activated at the same time.

    (Take engine activated = 1 engine Shut Down = 0)

    (i)   Obtain the truth table for this system.

    (ii)   Derive the sum of products (max terms) expression.

    (iii)   Implement the simplified function of system.

(7 Marks)

(c)   Draw the circuit for the function:

    $F = B + \overline{A}CD + \overline{B}\,\overline{D}$ using NAND gates only.   **(3 Marks)**

R ── (NOR gate) ── Q

Initial Condition
$Q = 0$
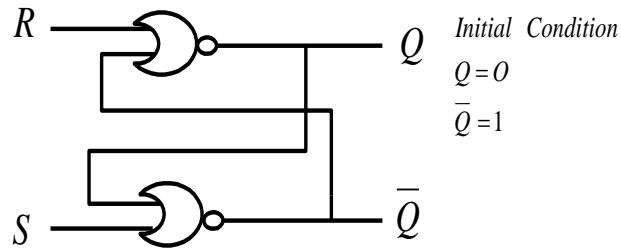$\bar{Q} = 1$

S ── (NOR gate) ── $\bar{Q}$

Fig. 1

Question THREE

(a)   With the aid of sketches explain the following terms as applied in logic families:

   (i)   Fan out
   (ii)   Propagation delay

(4 Marks)

(b)   (i)   Draw a logic circuit diagram of a Tri-state TTL Nand gate and
         explain its operation.   **(7 Marks)**

   (ii)   State **ONE** advantage and **ONE** disadvantage of ECL over TTL. **(2 Marks)**

(c)   (i)   Explain the operation of the circuit in fig. 2.

   (ii)   Describe the methods used to overcome the problem of floating
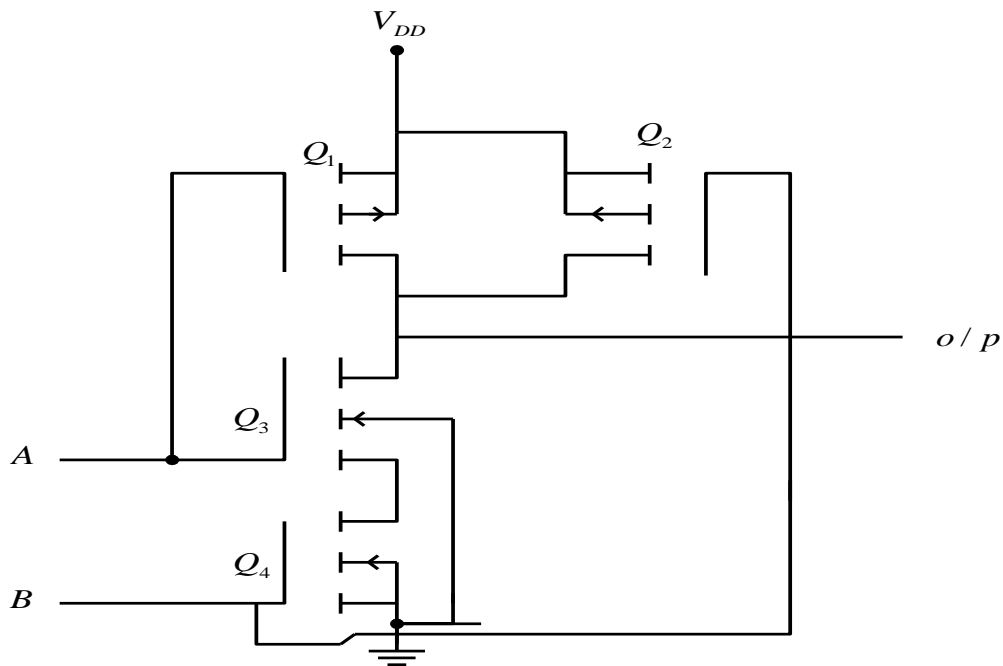   unused inputs.   **(7 Marks)**

Fig. 2

Question FOUR

(a)   (i)   With the aid of a logic diagram & truth table explain the operation of a J – K flip flop mentioning hw it differs from the S – R flip flop.

       (ii)   Discuss why the master-slave configuration is preferred to a standard J – K flip flop.

(9 Marks)

(b)   Use an appropriate sketch to distinguish between the set up time and hold time as applied in flip flop.   **(5 Marks)**

(c)   (i)   Show how S – R flip flop can be configured to form a D flip flop (latch).

       (ii)   Draw the:
           (I)   Truth table for the Flip flops in (i)
           (II)   Outputs the $QN\overline{Q}$ in fig. 2.

(6 Marks)

C/K

D

Q

$\overline{Q}$

Fig. 2

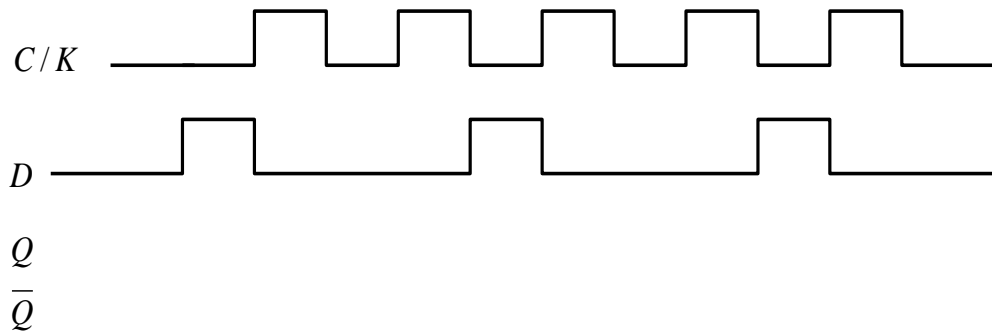### Question FIVE

(a)   Convert

       (i) 10011010.110_2 to decimal

       (ii) 365_8 to binary

       (iii) 239_{10} to Hexadecimal

       (iv) 110011_2 to Gray

                                                     (6 Marks)

(b)   Perform the following arithmetic operations:

       (i) $A21_{16} + 13B_{16}$

       (ii) $135 + 228$ in BCD

       (iii) $364 + 143$ in ex $-$ 3

       (iv) $110011 - 10011,$ using 2^S compliment.

                                                      (8 Marks)

(c)   State any **TWO** advantages and **ONE** disadvantage of:

       (I)   Gray code over straight binary

       (II)   BCD codes over straight binary

                                                     (6 Marks)