



THE MOMBASA POLYTECHNIC UNIVERSITY COLLEGE

Faculty of Engineering and Technology

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DEPE III

EEE 2203

DIGITAL ELECTRONICS II

SEMESTER EXAMINATIONS

SERIES: FEBRUARY 2011 SERIES

TIME: 2 HOURS

Instructions to Candidates:

Question ONE

- a) i) Construct a ripple counter having modulo 10.
- ii) Explain the operation of the circuit of fig 1.

Fig 1

- iii) State any ONE advantage and any ONE disadvantage of Johnson over ring counter. (10marks)

- b) i) Explain the term priority encoder.
- ii) With the aid of a logic diagram, explain how decimal to BCD encoding is achieved with OR gates only. (8 marks)

- c) i) Explain the difference between sequential access memory and random access memory.
- ii) State and explain any TWO types of read only memories (ROM).
- iii) Draw a diagram to show how 16 x 4 RAM can be connected to realize 16 x 8 RAM. (8 marks)

- d) A 10 bit DAC has a step size of 10mV, determine:
 - i) full scale output
 - ii) percentage resolution (4 marks)

Question TWO

- a) i) Write the aid of sketches, distinguish between asynchronous and synchronous counters.
- ii) State any TWO disadvantages of asynchronous counters. (4 marks)

- b) i) With the aid of a circuit and timing diagrams, explain the operation of a 4 bit shift register employing D flip flops. Assume the initial state is 0000 and data available at the input is 1011.
- ii) Draw a diagram of a 4 bit ring counter and explain its operation. (10marks)
- c) Design using J-K flip flops a synchronous counter to count through the states 1---2----5-----7 (6 marks)

Question THREE

- a) i) With the aid of a circuit diagram, describe how the two numbers 11101 contained in register A and 10101 in register B are added in a parallel adder.
- ii) Draw a block diagram to show how the full-adder may be realized from two half adders.
- iii) Design and implement a half subtractor. (16marks)
- b) With the aid of a block diagram, explain the operation of 4 to 1 line multiplexer. (4 marks)

Question FOUR

- a) Define the following terms:
- i) resolution
- ii) linearity
- iii) setting time (3 marks)
- b) i) With the aid of circuit diagram, explain the operation of a 4 bit binary weighted digital to analog converter and derive the expression of the output voltage.
- ii) State any TWO disadvantages of the converter in (i) above.
- iii) Outline the conversion steps on fig 2. (13marks)

Fig 2

- c) Determine for a 5 bit successive approximation analog to digital convertor the digital output corresponding to an analog input of 4.0625V given the reference voltage is 5V. (4 marks)

Question FIVE

- a) Define the following terms as applied to memories
- i) access time
 - ii) volatile (2 marks)
- b)
- i) State any ONE advantage and any ONE disadvantage of dynamic compared to static RAM.
 - ii) Describe the steps of writing data into memory location in the 16 x 4 RAM.
 - iii) Show how two 16 x 4 chips may be combined to form 32 x 4 memory. (12marks)
- c)
- i) Draw a logic diagram of a 2 to 4 line decoder
 - ii) Explain the function of the enable inputs in a decoder. (6 marks)