THE MOMBASA POLYTECHNIC UNIVERSITY COLLEGE

(A Constituent College of JKUAT)

(A Centre of Excellence)

Faculty of Engineering & Technology

DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY

UNIVERSITY EXAMINATION FOR:

BACHELOR OF SCIENCE IN INFORMATION TECHNOLOGY

(BSc. IT M111/12)

ICS 2205: DIGITAL LOGIC

END OF SEMESTER EXAMINATION

SERIES: DECEMBER 2012

TIME: 2 HOURS

Instructions to Candidates:

You should have the following for this examination

- *Answer Booklet*

This paper consist of **FIVE** questions

Answer question **ONE (COMPULSORY)** and any other **TWO** questions

Maximum marks for each part of a question are as shown

This paper consists of **FOUR** printed pages

Question One (Compulsory)

a) Highlight the characteristics of the decimal number system. **(4 marks)**

b) Perform the following operations:

(i) $0110_2 - 1000_2$ (Using the I's compliment)

(ii) $100.1B_{16} - OFF.OD_{16}$ (Convert your answer to decimal

(iii) $275_8 + 57_8$ (Convert your answer to hexadecimal) **(8 marks)**

c) Draw an electronic realization/equivalent of a NOT gate and explain its operation. **(5 marks)**

d) (i) Differentiate between a combinational logic and sequential logic.

(ii) Draw a logic circuit to implement a half odder, obtain the truth table. **(7 marks)**

e) Obtain a simplified expression for the K-map below and implement the simplified expression using logic gates.

Z \ AB	00	01	11	10
00	0	0	1	1
01	1	0	1	1
11	0	0	0	0
10	1	1	1	1

CD

(6 marks)

Question Two

a) Describe the binary number system highlighting its characteristics.

b) Perform the following conversions:

(i) 62510 to Hexadecimal

(ii) $3C8.23_{16}$ to octal

(iii) 110.325_{10} to binary **(6 marks)**

c) Perform the following arithmetic

$110100_2 \div 100_2$

(i)

$47_{16} - 37_8$

(ii)

$1101_2 \times 111_2$

(iii) leaving your answer in hexadecimal. **(6 marks)**

d) Perform the following logic operations:

11011_2 *and* 10010_2

(i)

$010101_2 \times 0R001010_2$

(ii)

100101_2

(iii) Determine the 2's compliment of **(4 marks)**

Question Three

a) Prove the following Laws of Boolean Algebra:

$A + \overline{A}B = A + B$

(i)

$A + BC = (A + B)(A + C)$

(ii) **(4 marks)**

b) For the logic circuit below (figure 1)

(i) Determine the expression for the output Z

(ii) Simplify the expression using Boolean Algebra

(iii) Implement the simplified expression using logic gates. **(8 marks)**

Figure 1

c) From the truth below:
   (i) Determine the expression for the output Y and simplify it.
   (ii) Implement the expression for Y using NOR gates only

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(8 marks)

Question Four

a) Describe a K-Map and explain how it can be used to minimize an output expression (Z) having three inputs m, n and p. **(7 marks)**

b) Simplify the following expression using K-Map and implement the simplified expression.

$$Z = \overline{\left(\overline{A+B} \bullet C\right)} + CA \bullet \overline{B+C}$$

(7 marks)

c) Determine the expression for the following K-Maps.

(i)

CD \ AB	00	01	11	10
00	0	1	0	0
01	1	0	1	1
11	0	1	1	0

10	1	1	0	1

(ii)

Z / AB	00	01	11	10
0	0	0	1	1
CD 1	1	0	1	1

(6 marks)

Question Five

a) (i) Describe how a multiplexer operates.

(ii) Write the expression for a 4-1 line demultiplexer and implement the expression using logic gates. **(6 marks)**

b) Differentiate between asynchronous and synchronous sequential circuits. **(4 marks)**

c) Draw a NAND gate realization of an edge triggered O flip flop and explain the operation of the flip flop. **(4 marks)**

d) Design a logic circuit with three inputs variables that will produce a "I" output when only two input variables are I's **(4 marks)**